

COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

OCTOBER 1977

MICROCOMPUTERS DECENTRALIZE PROCESSING IN DATA COMMUNICATIONS NETWORK

MICROCODE INCREASES MINICOMPUTER PROCESSING CAPABILITY

FLAT PANEL DISPLAYS OFFER GRAPHICS ALTERNATIVES



At last... a Logic State Analyzer that practically asks you what to analyze and how to display.

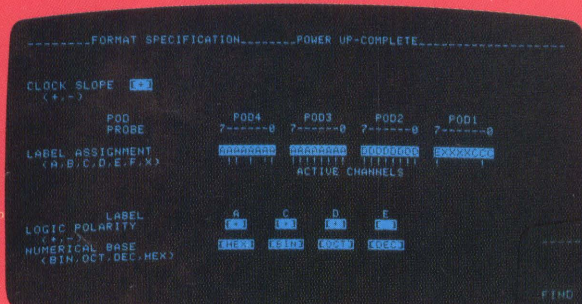
A few simple pushbuttons, an interactive display, sophisticated microprocessor-based intelligence... now they're all combined in HP's powerful new 1610A Logic State Analyzer. The result is a simplified "menu" approach to instrument setup, ability to choose highly complex trace specifications with a few simple keyboard entries, program-flow displays that are easier than ever to interpret, and an instrument that virtually self tests.

In addition, now you can trace complex branches and nested loops; count the number of states or the time

interval between all words to debug or optimize programming; and drive HP Model 9866A or 9866B printers for hard-copy output of test results and set-up specifications.

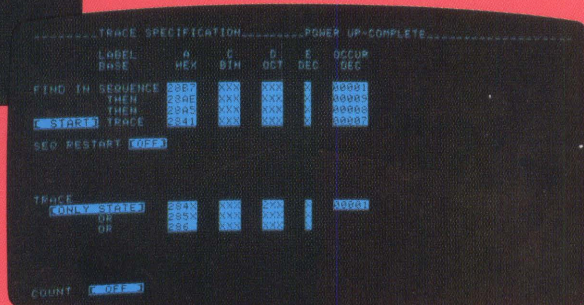
The new 1610A, priced at \$9500*, provides fast setup and easy trouble-shooting in nearly any logic system having data rates to 10 MHz. Your local HP field engineer has the complete story. Give him a call today.

* Domestic U.S.A. price only.



Setup ease. Inverse-video fields and moveable cursor in Format Specification mode direct you in defining clock slope, positive or negative logic and display formats (Hex, Binary, Octal or Decimal). You can also assign alphabetic labels to groups of data bits acting as a unit, greatly simplifying setups and display formatting. In addition, the display verifies probe-lead continuity and signals mode activity.

Complex measurement capability. Fields and moveable cursor in Trace Specification mode simplify selection of trigger conditions and trace qualifiers. The ability to define up to seven sequential 32-bit words makes it possible to trace a specific path in complex branched programs. For further conditioning you can define the number of times each sequential state is to occur to allow the analyzing of looped or nested loop programs. And you can define up to seven states or groups of states for selective trace, simplifying data analysis and reducing the need for deep memory.

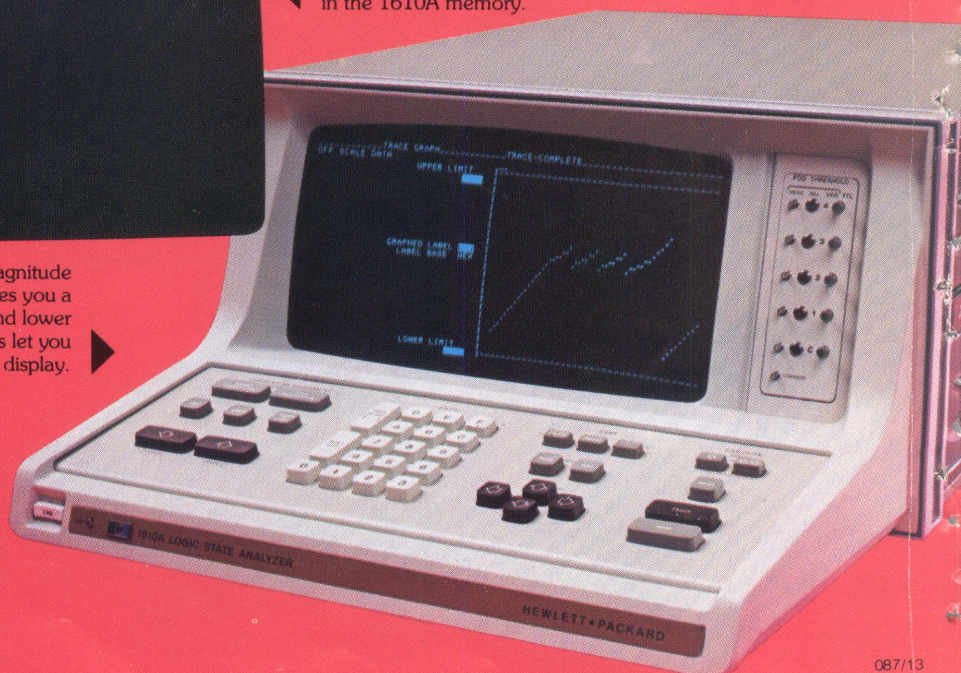



Simplified interpretation. List Display shows you trigger words plus the program flow you specified in the set-up specifications. Now you can easily compare operating software to original source listings or, in the trace-compare mode, to program flow stored in the 1610A memory.

Trace List mode display showing a list of states with their corresponding hexadecimal, binary, octal, and decimal values.

	A	B	C	D	E
SEQUENCE	28B7	11	286	0	
SEQUENCE	28AE	11	286	0	
SEQUENCE	2845	11	882	0	
START	2841	11	880	0	
+01	2842	11	233	0	
+02	2844	11	223	0	
+03	2846	11	288	0	
+04	284A	11	212	0	
+05	284C	11	204	0	
+06	2850	11	244	0	
+07	2851	11	010	0	
+08	2852	11	010	0	
+09	2852	11	010	0	
+10	2853	11	112	0	
+11	2853	11	112	0	
+12	2854	11	052	0	
+13	2854	11	052	0	
+14	2855	11	273	0	
+15	2851	11	010	0	
+16	2855	11	010	0	

System overview. Graph Display, showing data magnitude (y axis) vs. time for all 64 words in memory, gives you a system overview. Keyboard entries establish upper and lower y-axis scale values, and moveable intensified dots let you select specific areas for list display.



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- A position arm anticipatory sensing system. An exclusive Kennedy feature, the linear, non-contact (Mag Pot) position sensor requires no lamp source and assures performance for the life of the machine.
- Interchangeable electronics on all Series 9000 transports, reduce stocking costs and down time.
- Front-accessible off-line test panel; marginal skew check; threshold scanning which automatically compensates for drop-ins or drop-outs; Read-After-Write shortened skew gate; simplified tape path and quick-release hubs.

- All models are available with either 7 or 9 track, 800 NRZI, 1600 PE or 800/1600 NRZI/PE.
 - 7 and 9 track NRZI and PE format/ control units to simplify customer electronics. Also, a variety of popular mini-computer mag tape controllers are available.
- Series 9000's performance is as impressive as its features, with data transfer rates to 72KHz, and tape speeds from 10 to 45 ips. Series 9000 is the hottest digital tape transport series around, and we plan to keep it that way, with constant improvements, rigid quality control and greater service capabilities. That should give you a warm feeling if you have a requirement for digital tape transports.

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(213) 798-0953



KENNEDY-QUALITY-COUNT ON IT

CIRCLE 2 ON INQUIRY CARD

This Tally printer knows the shortest way to double or triple your throughput.

You get there faster if you don't have as far to go. Tally's Model T-1602 optimized bi-directional serial printer prints left to right and right to left while its microprocessor looks ahead for the shortest path to the next line of print. These short cuts add up fast to slash your throughput time by two to three fold. (Of course, throughput savings are tied directly to the amount of white space in your format.)

"Optimized" means moving the print head—left or right—to pick up the closest character on the next print line. There's no lost time with conventional carriage returns. And coupled with an 8-1/2 ips slew speed, the T-1602 moves the print head at an accelerated rate to the next print position. The print head moves at three times the print rate over blank spaces.

And remember, you get this bonus throughput without taxing the machine—the printing rate remains at 160 characters per second to achieve printing speeds of 70 to 200 lines per minute.

The Model T-1602 is the newest member of the T-1000 Series—Tally's fine line of serial printers that offer microprocessor electronics, low acoustic noise level, digitally controlled print head advancement, dual tractor engagement and a convenient snap-in ribbon cartridge.

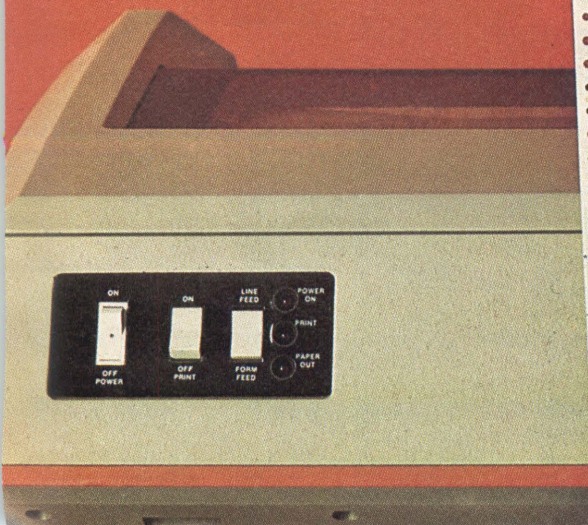
There's more to tell, so call your nearest Tally sales office.
Tally Corporation, 8301 S. 180th Street, Kent, WA 98031.
Phone (206) 251-5524.

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San Antonio (512) 733-8153
New York (516) 694-8444
Boston (617) 272-8070
Chicago (312) 325-9788
Miami (305) 665-5751
Seattle (206) 251-6730
Washington, D.C. (703) 471-1145
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TALLY

CIRCLE 3 ON INQUIRY CARD



TALLY T-1000 SERIAL PRINTER

THIS IS THE NEW TALLY T-1000 SERIAL PRINTER PRINTING AT 120 CPS UNDER THE CONTROL OF AN INTERNAL MICROPROCESSOR. IT'S HIGH RELIABILITY AND UNIQUE FLEXIBILITY BRING A NEW DIMENSION TO THE HIGH SPEED SERIAL PRINTER MARKET. EXCELLENT PRINT QUALITY, TRACTORS ABOVE AND BELOW THE PRINT LINE AND EASILY CHANGED RIBBON CARTRIDGE ARE ADDITIONAL FEATURES WHICH MAKE THE TALLY T-1000 IDEAL FOR USE IN YOUR DATA SYSTEM.

PRINT SPEED	120 CPS
PRINT WIDTH	132 COLUMNS
MATRIX	9 x 7
SLEW SPEED	7 INCHES PER SECOND
LINE SPACING	6 LINES PER INCH
PAPER WIDTH	4 TO 15.4 INCHES
RIBBON LIFE	1.5 MILLION CHARACTERS
VERTICAL FORMAT CONTROLS	
PRINT PSE PART 10000	

TALLY CORP., 8301 S. 180TH ST., KENT, WASHINGTON 98031 206/251-5500

TALLY T-1000 SERIAL PRINTER

THIS IS THE NEW TALLY T-1000 SERIAL PRINTER PRINTING AT 120 CPS UNDER THE CONTROL OF AN INTERNAL MICROPROCESSOR. IT'S HIGH RELIABILITY AND UNIQUE FLEXIBILITY BRING A NEW DIMENSION TO THE HIGH SPEED SERIAL PRINTER MARKET. EXCELLENT PRINT QUALITY, TRACTORS ABOVE AND BELOW THE PRINT LINE AND EASILY CHANGED RIBBON CARTRIDGE ARE ADDITIONAL FEATURES WHICH MAKE THE TALLY T-1000 IDEAL FOR USE IN YOUR DATA SYSTEM.

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OCTOBER 1977 • VOLUME 16 • NUMBER 10

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81 MICROCOMPUTERS DECENTRALIZE PROCESSING IN DATA COMMUNICATIONS NETWORK

by Donald J. Mueller

A microcomputer design approach to a complex data communications network offers localized data concentration, circuit switching, and diagnostic testing, and results in optimal task management at low cost

91 MICROCODE INCREASES MINICOMPUTER PROCESSING CAPABILITY

by Steven Buchwald

User-accessible microcode offers accelerated processing speed and faster execution of specialized instructions and common algorithms for modern minicomputers. These attributes can be implemented by understanding microprogramming techniques, application conformities, and control processor functions

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by G. E. King and A. V. Nelson

Stored photographic material, in microfiche format, is readily selected and projected by a mechanical viewer operating under digital electronic control

115 DIGITAL IMAGE PROCESSOR LINKS TV SIGNAL SOURCES TO COMPUTER

by Roger Dahlberg

Coupling TV signal sources to a computer, this digital interfacing system concept furnishes real-time video images for display and assists in reducing computer processing tasks

166 OPTICAL DATA ACQUISITION SYSTEM COMBINES VIDEO AND DIGITAL TECHNOLOGIES

Multispectral scanner and image digitizer capture spatially distributed scenic data, convert picture elements to 8-bit words, and transmit them to a storage device for later study

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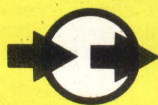
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CALENDAR

CONFERENCES

OCT 17-19—ACM (Assoc for Computing Machinery) Annual Conf, Olympic Hotel, Seattle, Wash. INFORMATION: Dr James S. Ketchel, PO Box 16156, Seattle, WA 98116. Tel: (206) 935-6776, (206) 623-4987

OCT 25-27—Semiconductor Test Sym, Cherry Hill, NJ. INFORMATION: Mrs R. J. Sunderland, Secretary and Registrar, Test Symposium Committee, PO Box 2340, Cherry Hill, NJ 08034. Tel: (609) 424-2400

OCT 27 and NOV 17—Invitational Computer Conf, Cabana Hyatt House, Palo Alto, Calif; and Houston Oaks, Houston, Tex. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: (714) 644-6037

OCT 28—Society for Information Display (SID) One-Day Technical Conf, Sheraton Inn/Airport, San Diego, Calif. INFORMATION: Dan Heflinger, Datagraphix, Inc, PO Box 82449, San Diego, CA 92138. Tel: (714) 291-9960

OCT 31-NOV 2—AIAA/IEEE/NASA Computers in Aerospace, Hyatt House Hotel, Los Angeles, Calif. INFORMATION: Hugh Harrington, Dept E411, McDonnell Douglas Astronautics, PO Box 516, St Louis, MO 63166. Tel: (314) 232-9102

OCT 31-NOV 2—18th Annual IEEE Sym on Foundations of Computer Science, Marriott Inn, Providence, RI. INFORMATION: Prof John E. Savage, FOCSS '77, Program in Computer Science, Box D, Brown U, Providence, RI 02912. Tel: (401) 863-2601

OCT 31-NOV 3—Computer-Aided Design and Computer-Aided Manufacturing Conf and Exhibit (CAD/CAM V), Cobo Hall, Detroit, Mich. INFORMATION: Society of Manufacturing Engineers, PO Box 930, Dearborn, MI 48128. Tel: (313) 271-1500, X403

NOV 1-3—INTERFACE WEST (Conf on Micros in Computers and Communications), Los Angeles Conv Ctr, Los Angeles, Calif. INFORMATION: INTERFACE WEST, 160 Speen St, Framingham, MA 01701. Tel: 1-800-225-4620, (617) 879-4502

NOV 2-4—AUTOTESTCON '77 (IEEE Internat'l Automatic Testing Conf), Dunfey's Resort, Hyannis, Mass. INFORMATION: Eugene B. Galton, Gen'l Chm, AUTOTESTCON '77, RCA Corp, PO Box 588, Burlington, MA 01803. Tel: (617) 272-4000

NOV 7-11—Electronic Components '77, U.S. Trade Ctr, London, England. INFORMATION: Robert Connan, Office of Internat'l Mktg, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-3465

NOV 8-10—Compec UK '77 (Computer Peripherals Exhibition), Wembley Ctr, London, England. INFORMATION: Iliffe Promotions Ltd, Dorset House, Stamford St, London SE1 9LU, England

NOV 8-10—MIDCON, O'Hare Conv Ctr and Hyatt Regency Hotel, Chicago, Ill. INFORMATION: W. C. Weber, Jr, IEEE, 999 Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965

NOV 8-10—Canadian Computer Show Conf, Internat'l Ctr of Commerce, Toronto, Canada. INFORMATION: Derek Tidd, Show Mgr, Industrial and Trade Shows of Canada, 481 University Ave, Toronto, Ontario M5W 1A7, Canada

NOV 8-11—23rd Annual Conf on Magnetism and Magnetic Materials, Radisson Hotel, Minneapolis, Minn. INFORMATION: D. C. Graham, Jr, Dept of Metallurgy and Materials, U of Penn, Philadelphia, PA 19174

NOV 8-11—COMPSAC '77 (IEEE Computer Soc Software and Applications Conf), Sheraton-O'Hare Motor Hotel, Chicago, Ill. INFORMATION: Prof Stephen S. Yau, Dept of Computer Science, Northwestern U, Evanston, IL 60201. Tel: (312) 492-3641

NOV 14-16—Distributed Data Processing Conf, Ramada O'Hare Inn, Chicago, Ill. INFORMATION: American Institute of Industrial Engineers (AIIE), Dept PR, PO Box

3727, Santa Monica, CA 90403. Tel: (213) 450-0500

NOV 15-17—6th Annual Meeting of Members of Computer-Aided Manufacturing—Internat'l (CAM-I), Americana Inn, Arlington, Tex. INFORMATION: C. H. Link, Exec Secretary and Gen'l Mgr, CAM-I, 611 Ryan Plaza Dr, Suite 1107, Arlington, TX 76011. Tel: (817) 265-5328

NOV 28—NBS and IEEE Personal Computing Conf, Nat'l Bureau of Stds, Gaithersburg, Md. INFORMATION: Paul Meissner, A219 Technology Bldg, Nat'l Bureau of Stds, Washington, DC 20234. Tel: (301) 921-3427

DEC 5-7—IEEE Internat'l Electron Devices Meeting, Washington Hilton Hotel, Washington, DC. INFORMATION: Susan Hinman, Courtesy Assoc, 1629 K St, NW, Washington, DC 20006. Tel: (202) 296-8100

DEC 5-7—Nat'l Telecommunications Conf (NTC), Marriott Hotel, Los Angeles, Calif. INFORMATION: NTC '77, PO Box 1250, Pasadena, CA 91109

DEC 5-7—Winter Simulation Conf, Nat'l Bureau of Stds, Gaithersburg, Md. INFORMATION: Paul F. Roth, B250 Technology Bldg, Nat'l Bureau of Stds, Washington, DC 20234. Tel: (301) 921-3545

DEC 6-8—Mini/Micro Computer Conf, Anaheim Conv Ctr, Anaheim, Calif. INFORMATION: Robert D. Rankin, 5544 E LaPalma Ave, Anaheim, CA 92807. Tel: (714) 528-2400

SEMINARS

OCT 19-21 and DEC 5-7—Computer Contract Negotiation, New York, NY and Washington, DC. INFORMATION: Ruth Dargis, Registrar, Act-Brandon Co, 437 Madison Ave, New York, NY 10022. Tel: (212) 421-4688

OCT 26-28—Effective Use and Application of Minicomputers; OCT 26-28—Distributed Processing with Minicomputers; and OCT 31-NOV 2—Design of Online Systems, New York, NY; Phoenix, Ariz; and Kansas City, Mo. INFORMATION: Registrar, Institute for Advanced Technology, Control Data Corp, 6003 Executive Blvd, Rockville, MD 20852. Tel: (301) 468-8576

OCT 26-28 and NOV 2-4—Data Communications: An Introduction to Concepts and Systems; NOV 17-18—Data Communications: Advanced Concepts and Systems; NOV 17-18—Minicomputers and Microcomputers—Selection and Usage Guidelines, New York, NY; Chicago, Ill; Washington, DC; and San Francisco, Calif. INFORMATION: Peggy Quinn, Datapro Research Corp, 1805 Underwood Blvd, Delran, NJ 08075. Tel: (609) 764-0100, 1-800-257-9406

OCT 31-NOV 2—Microcomputer Interfacing Workshop, and NOV 14-18—ECM and ECCM for Digital Communication, GWU Tidewater Ctr, Hampton, Va. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

NOV 7-11—Online Network Systems: Trends in the 1980s, NOV 9-11—Data Base Systems in a Network Environment; and NOV 16-18—Distributed System Design Workshop, San Francisco, Calif; and Chicago, Ill. INFORMATION: American Institute of Industrial Engineers (AIIE) Seminars, Dept PR, PO Box 3727, Santa Monica, CA 90403. Tel: (213) 450-0500

SHORT COURSES

OCT 26-28, OCT 31-NOV 4, AND NOV 14-18—Hands-On Microprocessor Short Courses with Free Take-Home Microcomputer; and Hands-On Interfacing Workshop, Palo Alto, Calif; San Diego, Calif; and Indianapolis, Ind. INFORMATION: Jerilyn Williams, Wintek Corp, 902 N 9th St, Lafayette, IN 47904. Tel: (317) 742-6802

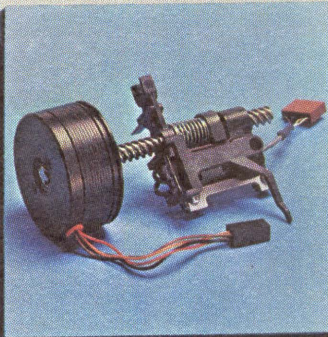
NOV 7-10 and NOV 14-17—F8 and F6800 Microprocessor Training Courses, San Jose, Calif. INFORMATION: John Hatch, Fairchild Camera and Instrument Corp, Instrumentation and Systems Group, 1725 Technology Dr, San Jose, CA 95110. Tel: (415) 962-3617

NOV 14-15—Minicomputer Programming and Interfacing Techniques, and NOV 16-18—Engineering Applications of Minicomputers, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

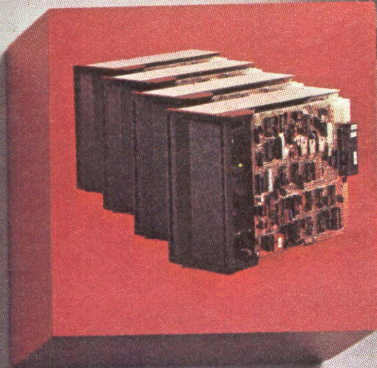
WANGCO: FIRST WITH ADVANCED TECHNOLOGY IN 5¼" DISKETTE DRIVES.



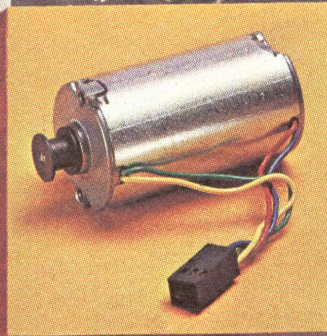
Data capacity to 498.8 Kbytes on one 5¼ inch diskette is achieved by exclusive 40 track recording, plus double density, plus dual sided recording. Dual index and file protect sensors permit recording on both sides of media.



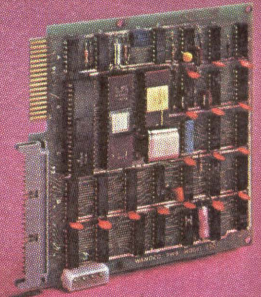
Fast access of 30 ms track to track is made possible by a low inertia, low friction, four-start lead screw positioning system, a field proven, high accuracy positioner technology.



Four-drive daisy chain capability with unit select provides up to 2 Mbytes data capacity in a convenient system configuration. Overlap seek speeds system access.



A precision, DC drive motor results in power dissipation of only 15 watts operating and 6 watts standby. No AC power is required, therefore, the Micro-Floppy Disk Drive functions conveniently worldwide.



Wangco's 5½" square, LSI based intelligent Micro-controller mounts on the Micro-Floppy Disk Drive providing a soft-sectored, IBM type format for up to four drives. Based on the Intel MCS 8048 micro-processor, the controller has a nine macro-command structure including diagnostic and automatic diskette copy. Most overhead requirements are greatly reduced.

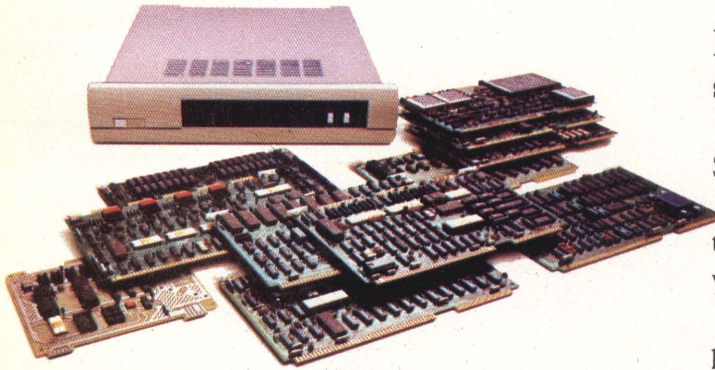
Look at all the features. Wangco's Model 82 Micro-Floppy Disk Drive clearly sets the standard in 5¼ inch diskette drives, including cast mainframe, ceramic ferrite head, photoelectric write protect, operator interlock and data reliability of 1 in 10⁹. Get full information from Wangco, Inc., 5404 Jandy Place, Los Angeles, California 90066. (213) 390-8081. In Europe: P.O. Box 7754, Building 70, 1st Floor, Schiphol-OOST, Netherlands. Phone: (020) 458269. TWX: 844-1882 WANGCO NL.



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SBC 80/20	8080A	2K	8K (2716) 4K (2708)	Multimaster
SBC 80/10	8080A	1K	4K (2708)	Single master
SBC 80/05	8085	512	4K (2716) 2K (2708)	Multimaster
SBC 80/04	8085	256	4K (2716) 2K (2708)	None

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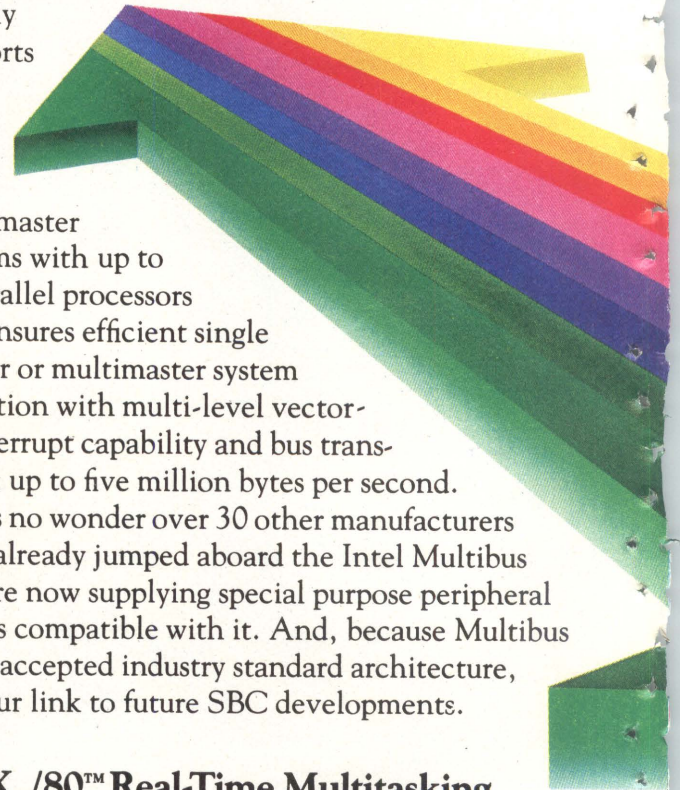
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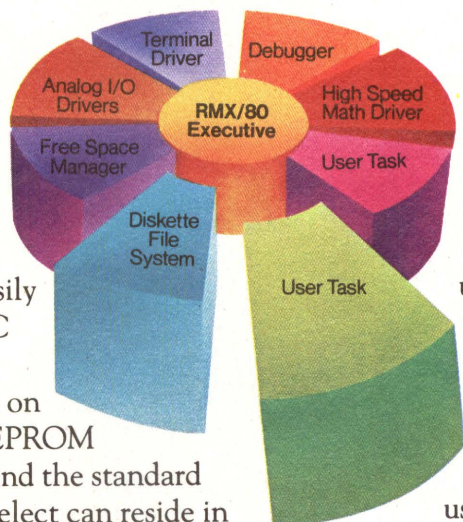
RMX/80 is the most advanced multitasking operating system for any Single Board Computer. For applications that monitor and control a number of interrelated asynchronously occurring events, it can dramatically cut software development time and costs. You develop software only for the individual tasks of your application, and the RMX/80 operating system does the rest providing all intertask communications and



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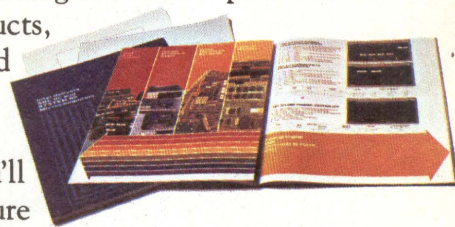
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by **John E. Buckley**
Telecommunications Management Corp
Cornwells Heights, Pa.

Data Communications Consultants

As a technology and its associated applications become more complex, independent expertise typically emerges. In the field of data communications and information systems, a virtually endless list could be compiled of individuals and organizations who profess to provide varying degrees of proficiency in the art of communications consulting.

Equipment and system manufacturers, suppliers, and users, as potential consulting clients, must first examine this resource to determine whether it would be a blessing or curse. Three factors which can cause divergent reputations are the selection of the consultant for the stated requirement; the compatibility between expected and actual results; and the ultimate acceptance of the original fee agreement. The proper understanding of these factors at the beginning of the client/consultant relationship will result in a positive experience. Guidelines can be developed to achieve this goal.

Professional consulting can be a catalyst in the advancement of technologies, as long as its utilization is selectively applied. Each manufacturer, distributor, and user, in isolated environments, tends to become stagnant in his views and applications of data communications technologies, perpetuating the traditional understandings and applications of that specialization. Fresh thinking is sometimes stimulated by new experienced employees; however, established employees usually evaluate this input with respect to their traditional concepts and may tend to discard it.

When and why the potential client decides that an independent consultant is necessary is a critical point. The decision is frequently based on reaction rather than anticipation; undesirable events involving economic or time constraints may stimulate management to reach for envisioned immediate relief—in the form of a consultant. The choice of consultant is usually first come-first selected. In such a situation, the client's own technical personnel view this decision as an indication of their management's loss of confidence in their capabilities, resulting in a defensive attitude which handicaps the effectiveness of even a competent consultant.

Management should attempt to anticipate the need for a consultant at the onset of a project rather than expecting

the consultant to cure some long-term situation. If a continual need for a particular expertise is foreseen, the proper solution is employment of competent personnel. For a consultant to provide continual expertise to relieve the hiring of personnel is unworkable from both economic and operational viewpoints.

Initially, the consultant envisions a long-term revenue source while the client believes that the consultant will function more efficiently and effectively than the addition of knowledgeable personnel. In the final analysis neither objective is realized. A consultant, serving many clients, takes longer to complete a single task than comparable client personnel. The consultant's time and attention are always directed at a multitude of actual or potential revenue sources. Therefore, a consultant should be used only in two cases: to satisfy an occasional one-time specialized knowledge requirement, and to provide a monitoring source (a form of checks and balances) with the client's technical staff.

A consultant's activities are always task- not objective-oriented. Once initiated, his services are seldom guided; a desired task is defined and the consultant is authorized to proceed, so that subsequent changes in the task are not easily accommodated. The properly performed task, however, may not meet the broader objectives planned by the client. This difference in perspective is the most common cause of a deteriorated client/consultant relationship.

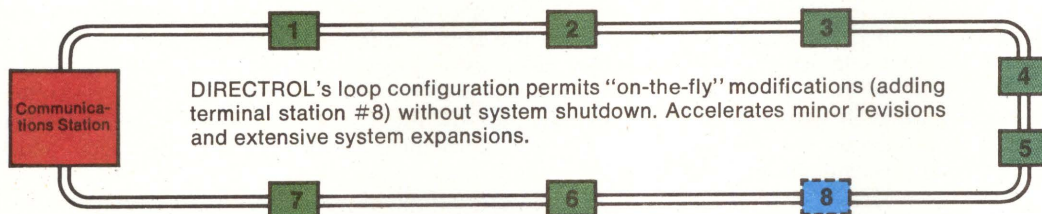
Every organization involved in a complex and dynamic technology, such as data communications, should maintain and update a dossier of competent consulting resources. Since it is unusual to find an individual who has expertise in all aspects of data communications technology, the precise area of concentration (such as software, applications programming, computer and terminal hardware, networks, protocols, tariffs, and regulations) should be designated in the listing. Depending on the nature of the consulting needs and the peripheral areas involved, a number of different consultants may be required.

The client must also identify the level of consulting service that is necessary—system planning, management, development, implementation, or operation. Each necessi-

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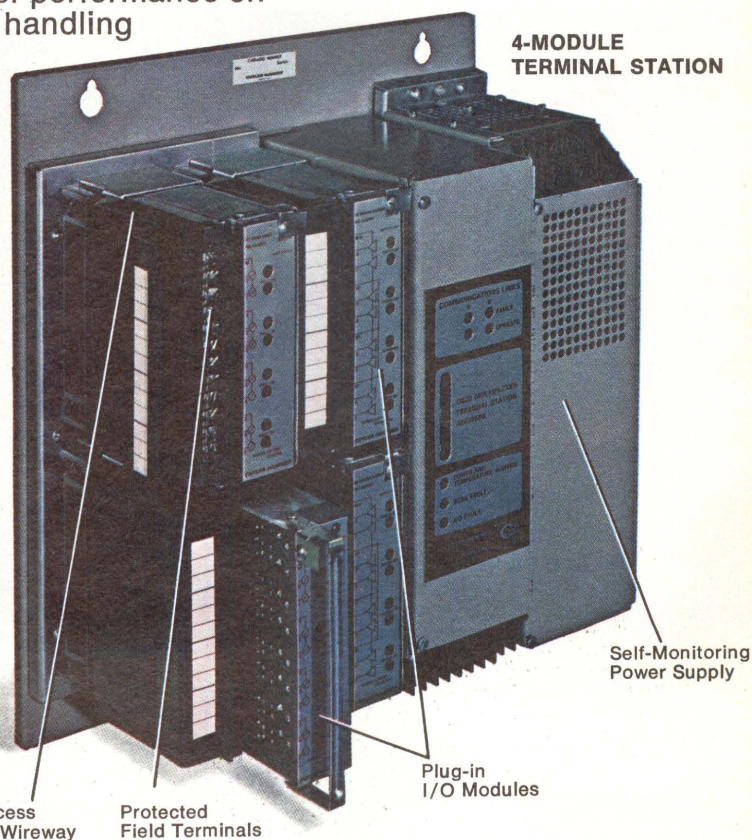
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tates a different consulting perspective. A negative client/consultant relationship can emerge when the selection of expertise was correct, but the level at which the consultant addressed the requirement (eg, development) was different from that required by the client (eg, planning). Perhaps the greatest need, which is the least realized, in this technology is for a consultant who consults on the selection of consultants.

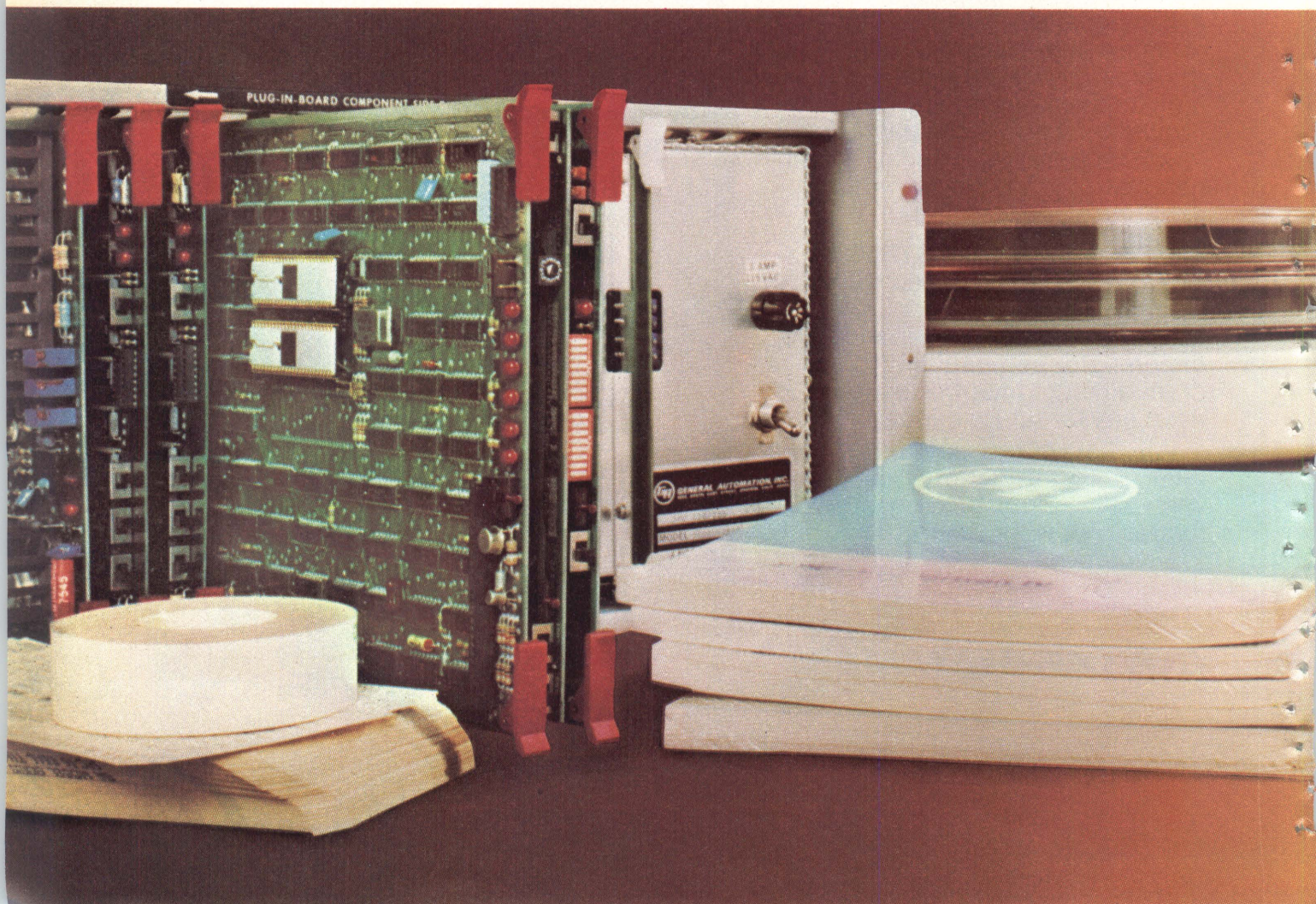
Once a consultant has been decided upon to assist in a specific area, there is a universal tendency to restrict his participation to sporadic problem discussion and evaluation sessions. Somehow this scattered participation is viewed as the lowest cost method of instilling knowledge and insights into the client's personnel, thereby providing the actual solutions from within. Exemplified by technical group therapy meetings, this occasional infusion of knowledge leaves all but the competent consultant with the belief that they have been regenerated with new insights and information, when in reality most of the advice is misleading and/or erroneous due to the misconceptions hastily conveyed to the consultant by the client's personnel.

While rarely practiced, the proper long-term and generalized association with a consultant should start at the beginning of a project, even if the actual need for such a consultant may not occur until the project is well underway. His participation or attendance in initial project planning meetings insures proper understandings of tasks and objectives, and results in the client's obtaining important input and guidance during the critical planning stages.

It is important that client and consultant have the same understanding as to the scope of the consultant's role, which may be either advisory or functional. If an advisory role is established, the consultant cannot be held culpable for a project error or problem unless his advice was a direct causal factor, and even then the client must confirm that the consultant had the proper project understanding. With a functional role (ie, a critical path activity), the client must provide the consultant with the same support that would normally be provided to any other project level manager.

In general, the use of a consultant in a direct project role without corresponding client personnel control and involvement is rarely satisfactory, usually concluding with a great deal of distaste for both sides. A consultant's most effective use is in a continual project monitoring and advisory role, with specialized tasks kept to a minimum. Ideally, such tasks would be directed by the consultant and executed by the client's personnel. The consultant should also participate in the problem definition which he is to subsequently address.

Consultants are often sought to solve an operational problem whose roots were well established during the initial planning stages of the project. Unable to effect a permanent, quick cure, the consultant ends up with a dissatisfied client. An equally common misuse is the client's changing the operational environment after the consultant has begun to perform an assigned task. For instance, a corporation once assigned a consultant to design a data communications network that could be shared by many individual data communications



applications; the desired objective was to realize a combined lower communications cost. While the network design task was in progress, the corporation reorganized its data communications applications to organizationally take advantage of this common network. The finished network design demonstrated that the desired communications economics were not applicable to all of the applications, which resulted in a dissatisfied client and an unreasonably maligned consultant.

Three methods of providing consultant compensation are per diem, retainer, and contingency. The typical per diem rate charged today for a qualified data communications consultant ranges between \$320 and \$600/man-day, equal to \$40 and \$75/hour. Higher rates must be commensurate with a highly unusual level of expertise; lower rates are usually an indication of minimal competency. If a guaranteed minimum number of hours per month is provided by the client, a 10 to 15% reduction is usually negotiable.

The monthly retainer fee is usually based on a one week/month minimum charge with the right to renegotiate on a 3- to 6-month basis. Such retainers do not guarantee that any specified amount of time will be applied to the client's requirements.

Contingency fees are usually found in existing problem situations, in which the consultant performs the necessary tasks to achieve a desired objective for a percentage of the improvement. For example, the consultant may agree to redesign a data communications network for 50% of the first year's network cost reduction. The client must realize that the consultant will insist on a projected savings

measurement which assumes that data terminal population and transmission volumes will remain constant for the fee-related year. These fee arrangements always result in significant revenues to the consultant and often a severely constrained network or system for the client. It must be remembered that the consultant is the expert, and he will not consider a contingency arrangement unless it is overwhelmingly advantageous. In most situations, the consultant's actions and recommendations become fee-oriented rather than client-oriented.

In all fee structures, all peripheral expense such as travel and living, telephone, and often office services such as typing and duplicating are additional. The client should establish clear budget guidelines with a consultant at the initiation of their relationship. Frequent and itemized invoicing must be demanded by the client. Many times a project will require intense additional participation by the consultant. When this activity is eventually billed by the consultant, the client has forgotten the demands of that situation and is reluctant to accept these charges.

Consultant expertise is a valuable resource that can be used or misused. A consultant must be a continually applied resource, not merely an occasional cure or corrective measure. His primary role is to monitor and advise, stimulating creativity in the client's technical staff, not replacing it. It is the client's responsibility to assure that the consultant is always attuned to the desired objectives and the associated operational environment. While not inexpensive, with the proper operating and management environment, a consultant can truly be a bargain for the client.

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Multichannel Subsystem Achieves Low Cost Communications

Complete computer hardware systems with multiple communications channels can be implemented at low cost with two plug-in circuit boards. This economy is achieved through the use of the SBC 534 4-channel communications expansion board, a flexible data communications subsystem, which has been added to the SBC 80 single-board computer family by the OEM Computer Systems Group of Intel Corp's Microcomputer Div, 3065 Bowers Ave, Santa Clara, CA 95051 (see *Computer Design*, "Micro Processor/Computer Data Stack," Mar 1976, pp 116, 118 and Nov 1976, pp 144, 146).

Containing mainly programmable LSI devices, the board has four serial i/o channels built around the 8251 programmable communications interface device—a software configured and controlled USART, which is fully duplex and incorporates parity, overrun, and framing error detection. Each channel has a separate baud rate generator based on the 8253 programmable interval timer, which provides any frequency from 18.75 Hz to 614.4 kHz. Two are contained on each board, each with three timers with 16-bit programmable counters. Auxiliary timers can generate real-time interrupt intervals of 1.63 μ s to almost 1 h. As rate generators they provide frequencies from 0.0029 Hz to 614.4 kHz. All channels also contain programmable digital loop-back for diagnostics. Each channel provides half- or full-duplex operation and contains an RS-232 interface and sockets for optically isolated, 20-mA current-loop interfaces. Each channel's operating modes (synchronous or asynchronous), data formats, and other functions are also individually programmable.

Lower costs/computer are also achievable with the subsystem; since all basic functions are software programmable, the same communications board can be shared by multiple SBC 80 computers containing the company's Multibus™ arbitration and control logic. Cost/channel can be reduced by using any number of SBC 534 subsystems with one or more SBC 80 or System 80 packaged OEM computers.

The board also contains buffered RS-232-C interface for the Bell 801 automatic calling unit (also usable

as 16 lines of general-purpose, RS-232-C interface); interface controls for auto-answer and auto-originare modems; and 16 levels of programmable interrupt control. USARTs, timers, parallel i/o, and interrupt controllers are configured as a block of 16 i/o addresses, which can begin at any 16-byte i/o address boundary.

Transmission rates/channel range up to 9600 baud in asynchronous operation and up to 38,400 baud in synchronous mode. Baud rates are derived from an onboard crystal oscillator. Channels can be programmed for most data communications protocols, including IBM Bisync. All registers in the programmable devices can be accessed in 400 ns.

Since the i/o subsystem built into the basic SBC 80 board is also programmable, a minimum 2-board system can be used with many types of modems, terminals, cassettes, and other peripherals, as well as with many control and instrumentation devices, with simple changes in applications programs. This concept is supported by the company's system software and the basic board designs.

The board operates on standard 5-, 12-, and -12-V power supplies, with 1.9 A, 275 mA, and 250 mA dc max, respectively. With optoisolators installed, the 5-V current remains at 1.9 mA, and the other two are 420 and 400 mA max. The board is priced at \$650 in single-unit quantities; volume discounts are available.

Circle 400 on Inquiry Card

SDLC Support Enhances Series of Programmable Terminal Systems

A synchronous data link control (SDLC) protocol enhancement has been added by Raytheon Data Systems Co's Communications Dept, 1415 Boston-Providence Tpk, Norwood, MA 02062, permitting PTS-100 systems to perform functions of remote IBM 3270 equipment communicating with a host mainframe under IBM's SDLC. Data can be sent and received simultaneously over a single communications line, for potentially lower line costs. Up to 40% of the cost of remote terminal equipment can be saved by users who have upgraded central site hardware and implemented teleprocessing systems needed to support the protocol.

Based on an 8-bit microprocessor, the communications adapter provides an interface between control units and modems with speeds ranging from 2k to 9.6k bits/s. Meeting standard RS-232-C modem interface requirements, it performs tasks such as zero insertion and deletion, and frame check sequence generation and checking for SDLC operation. Computations are performed in firmware relieving the control unit of that function.

Required software resides in 4k words of mos memory on the adapter board, allowing easy reprogramming of the adapter. The adapter plugs into a low speed multiplexer port in the terminal control unit, permitting current systems to be upgraded; only a tape cassette with remote 3271 SDLC emulator software and the adapter to replace the BSC modem adapter are necessary.

The SDLC communication provides increased flexibility while enhancing communications throughput and central site control. It has been tested online under such software systems as DOS/VM, VTAM, and NCP/PEP, in parallel with IBM 3270 equipment. Circle 401 on Inquiry Card

Downline Software Loading Aids Distributed Network Control

For effective, centralized management control of distributed data processing network operations, Computer Automation's Commercial Systems Div, 18651 Von Karman, Irvine, CA 92713 has announced a downline software loading capability for users of their SyFA network processing systems. Available at no extra charge on those systems, the feature permits transmission of applications programs and systems software throughout a distributed network from a designated central location. It is accomplished via a synchronous remote job entry link under IBM 3780 protocol.

Benefits include faster distribution of software as it is developed (transfer occurs at line transmission speeds), assurance of synchronized implementation of software by all computers in the network, and facilitating of recovery procedures from the central computer if data loss occurs at a remote site. Additional security against failures and fires is provided. Circle 402 on Inquiry Card

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The success of the Voyager projects will be measured by the ability of scientists to track and monitor the activities of the spacecraft and process the vital data returned to Earth. These critical functions are primarily performed for Voyager and other ongoing space missions, including Pioneer, Viking and Helios, by a series of MODCOMP computers in the Deep Space Network of Jet Propulsion Laboratories in

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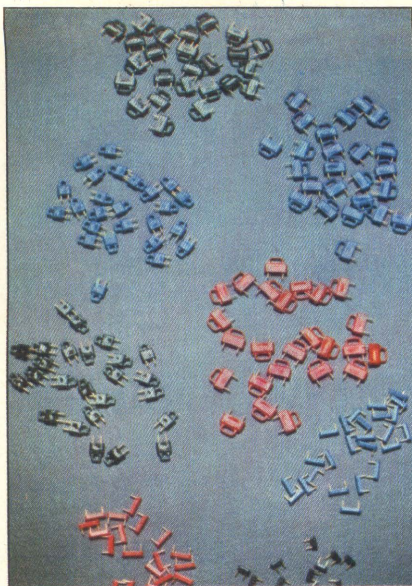
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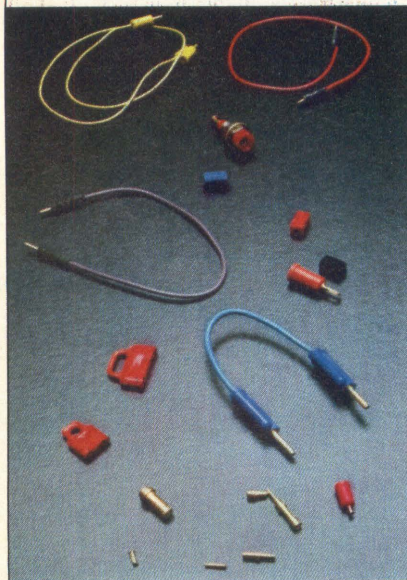
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Hawaii Is Planned As Next Extension of Packet Switched Service

Telenet Communications Corp, 1050 17th St, NW, Washington, DC 20036 and the Hawaiian Telephone Co have filed a joint application with the FCC seeking to extend the Telenet packet switched service for data communications to Hawaii, beginning in the fall. The service will be available on a demand basis with rates based on the volume of data exchanged.

Trans-Pacific cable facilities will connect the Continental U.S. network with the telephone company's operating center in Honolulu. Both carriers support the CCITT X.25 packet mode interface for synchronous and asynchronous communications.

A tariff submitted with the application sets charges at \$4/1000 packets, with each packet containing up to 128 characters of user data. Dedicated facilities at monthly rates will be offered for asynchronous transmission for 75 to 1200 bits/s and for X.25 synchronous transmission up to 9.6k bits/s.

Network Architecture Expands Application of Computer Systems

To lessen the workload and demand on the host computer and minimize cost of extra lines and duplicated programming, Fujitsu Ltd, Communications and Electronics, 6-1 Marunouchi 2-chome, chiyoda-ku, Tokyo 100, Japan has developed the Fujitsu Network Architecture (FNA). The logically structured and streamlined family of online computer networks features standardized components and high level data link control (HDLC) procedures.

Each network is made up of host computers, communication processors, subhosts, cluster controllers, and compatible terminals which are combined under a single-line discipline. Basically, data communications and data processing functions are separated within the system, enabling many applications to be accomplished on one line. Protocols and operational sequences are defined for transmitting information units through the system.

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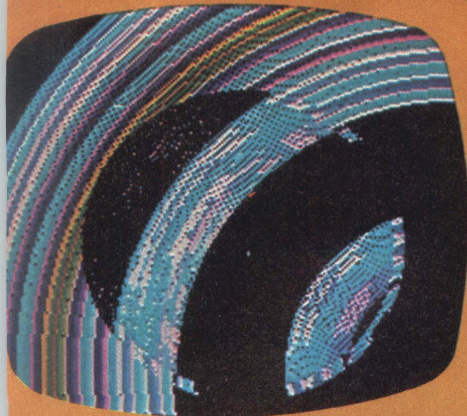
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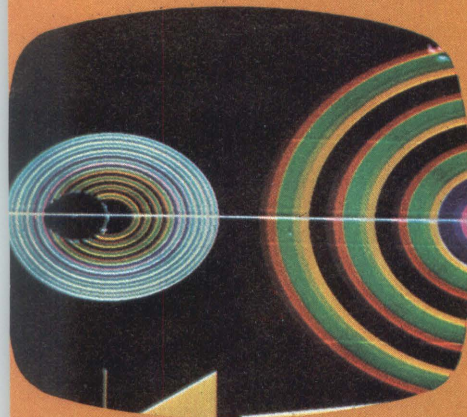
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A color display system with 512 x 512 resolution at a 60 Hz repeat field refresh rate. For the first time 512 flicker free lines in full color can be resolved. The Aydin Model 5214FS Display Generator eliminates flicker by outputting data at twice the conventional rate to the Aydin Model 8023 Ultra High Resolution 19 inch color CRT Monitor. A flicker free display is provided while still maintaining full image and graphic generation capability. The Model 5214FS provides vector, circle and character generation in addition to color look-up tables.

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COMMUNICATION CHANNEL

HDLC procedures; other transmission control procedures are also available. Access is provided to leased lines, telephone switching systems, Dendenkosha Data Exchange, data highway, and optical communications. Based on recommended guidelines of the ISO and CCITT, the FNA is compatible with all networks in or out of Japan. It incorporates the M series network architecture, and is therefore scheduled to align with the data communications network architecture.

Circle 403 on Inquiry Card

Future Communications Capabilities Are Explored In Satellite Experiment

An advanced communications experiment, known as Project Prelude, will use the Communications Technology Satellite (CTS) launched in 1976 to test emerging concepts for intracompany communications including high speed data transmissions, teleconferencing, and facsimile. Satellite Business Systems (SBS), 8003 Westpark Dr, PO Box 908, McLean, VA 22101 will conduct the project during the fourth quarter of 1977 in association with Comsat Laboratories.

Two Comsat small transportable earth stations will be installed for several weeks at sites selected by Rockwell International Corp, Texaco, Inc, and Montgomery Ward and Co, Inc, who are participating in the experiment. Various communications equipment manufacturers are to supply terminal equipment at each of the sites. Approval for the experiment has been received from the FCC and NASA, which operates the CTS satellite in conjunction with the Canadian government.

The experimental transmission will be at 12- and 14-GHz frequencies at which the CTS operates; it will serve to introduce the advanced commercial communications which will be available in the 1980s to meet intracompany needs of large organizations. It will also provide an opportunity to plan, develop, and evaluate equipment in a business environment for high speed and high quality transmission capabilities required for future satellite systems.

Data are to be gathered on user acceptance, economic impact, and equipment performance. An evaluation will be published in a report to

NASA and the FCC. SBS has also been authorized by the FCC to establish a digital 12/14-GHz satellite system, planned for commercial operation beginning January 1981, which will provide switched, private networks for users with small earth terminal sites.

Packet Switching Network Is To Be Built In The Netherlands

A minicomputer-based packet switching network is to be built by Logica Benelux BV—sister company of Logica, Inc, 801 Second Ave, 13th Floor, New York, NY 10017—for the Rijkswaterstaat (Water Control Dept of the Dutch Ministry of Transport and Public Works), The Netherlands. The communications network (CNET) is expected to service existing local and remote terminals by mid-1978, and to provide communications between several Dutch ministries' networks through the planned national packet-switched network of the Postal Telephone and Telegraph by 1979/80, enabling sharing of existing large computer facilities.

Based on the European Informatics Network of switching nodes, CNET handles all communications protocol conversions, requiring no modification of existing mainframe operating systems or hardware. The CCITT X.25 protocol incorporating virtual call service will be implemented.

Five DEC PDP-11/34 minicomputers with 48k words of core memory and communications interfaces will be used—three will function as host interface processors (HIPs) for the central mainframes, and two as switching nodes to low and medium speed terminals, connecting to two of the HIPs. Connections will be over 48k-bit/s lines.

Data Communications Products Are Suited To Advanced Applications

Several products—a programmable communications processor, advanced software system, and computer peripherals—have been announced by Comten, Inc, 1950 W County Rd B-2, St Paul, MN 55113 for use in advanced data communications applica-

Remex launches a PDP-11 floppy disk system with above DEC performance



It's an integrated hardware/software system so compatible with DEC's RT-11 operating system that we named it Remex-11.

It connects directly to the PDP-11 or LSI-11 bus, offers about 25 percent greater storage capacity than Digital's RX11 disk system, and it costs less.

In addition, the Remex-11

provides faster throughput than standard DEC configurations with more efficient sectoring, by far. A single command transfers up to 65K words.

A full array of switches and indicators makes operation easy.

If you're a PDP-11 user, set sail for Remex. High quality peripherals and their

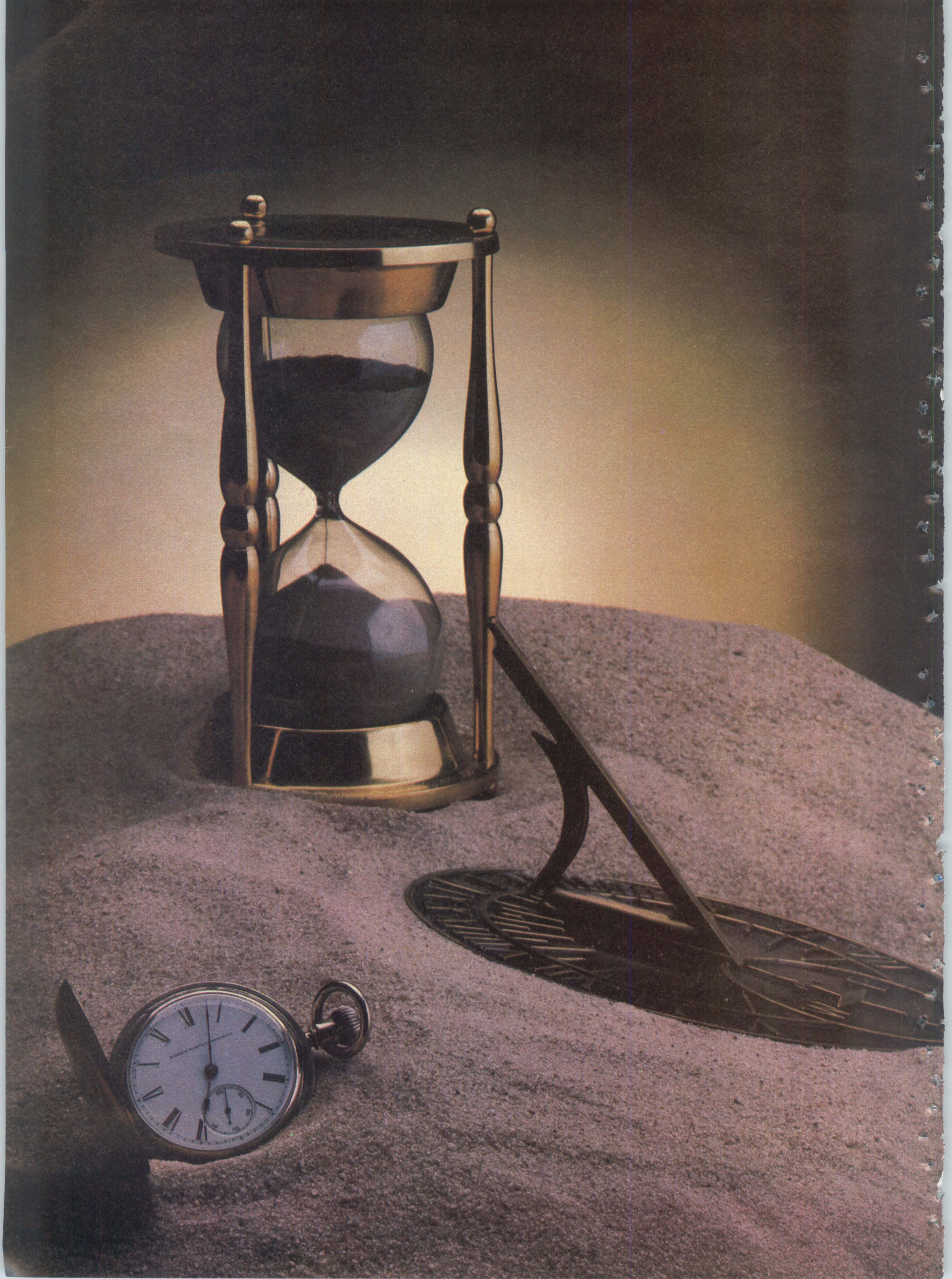
service are our only business. If you've bought any of our more than 100,000 punched tape and flexible disk units, you know what we mean.

Contact your nearest Remex Sales Office or the factory direct: P.O. Box C-19533, 1733 Alton St., Irvine, CA 92713. Phone: (714) 557-6860

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REMEX DIVISION

CIRCLE 16 ON INQUIRY CARD



Real-time problems? Systems has timely solutions.

Systems Engineering Laboratories has dedicated its 16 year corporate life to solving challenging real-time problems. The experience gained in solving these problems is what led us to pioneer the development of true 32-bit computer systems.

Look into the operating systems, the languages, the data base system, the real-time device handlers and terminal systems, and you will see that we build for the real-time environment. That's our business.

Choose from a well-bred family of computing systems: The SEL 32/35, the SEL 32/55, or the SEL 32/75. Unlike other so-called "32-bit minis" that are only bridge-the-gap systems developed from essentially 16-bit architecture, all SEL 32 systems are true 32-bit machines. This results in richer instruction sets, more precision in data representation and larger, directly-addressable memory. All are available with throughput rates in excess of 26 million bytes/second.

Systems computers fit the term "minicomputer" in price alone. If your application is performance-sensitive, we'll save you money. If you're budget-sensitive, we'll give you more performance for your dollar.

The SEL 32/35 can be configured from 64K bytes to 512K bytes of 900 nsec memory. Resembling its more powerful brothers, the SEL 32/35 is a complete package, including control processor with floating-point arithmetic, memory, chassis, power supplies and cabinet.

The SEL 32/55 is offered in a variety

of both single and multiple CPU configurations, with from 32K bytes to 1 million bytes of 600 nsec memory.

The SEL 32/75, with up to 16 million bytes of main memory, has a concept so new, we had to coin a special term to describe one of its main features: Regional Processing Units. Working independently, these RPU's contain sufficient control and buffer storage areas to process an I/O region and transfer the resultant data directly to main memory. Computer system throughput is further enhanced by High-Speed Floating-Point Hardware and Writeable Control Storage.

Just circle our number on the Reader Service Card, or call us today. We'll send you the powerful story of the SEL 32 family.

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tions. The processor is a medium- to large-scale device; the software system is a processing and control system for distributed networking; and the peripherals, including tape, disc, and unit record equipment, provide i/o for processors using the software system.

Communications Processor

While maintaining upward compatibility with the company's 3650 II and 3670 II processors, the 3690 has been enhanced, executing instructions five times faster, and attaching to four times more communications lines. Features are multiple-host support for up to eight IBM host computer systems, line facilities for up to 512 full-duplex communications lines, and support for IBM and non-IBM terminals. With an expanded instruction set, the unit uses microprocessing with a wide microword to preset hardware functions. Overlapped instruction execution uses lookahead techniques.

Also featured are a main storage system with dual 32-bit wide bank-access paths; dual register sets;

control registers, varying up to 32 bits in length; and an i/o structure that allows independent channel programming on all communications and peripheral i/o interfaces. Installation and maintenance aids are also included.

Available in several basic configurations for host frontend, remote terminal concentration, and stand-alone data processing, the processor performs advanced network services such as satellite communications and data switching.

Software System

The Data Switching System (DSS) enables use of the 3650 II, 3670 II, and 3690 processors for host frontend processing, remote terminal concentration, and data switching to distribute those functions to desired network nodes. Capabilities of the first two releases (1 and 2) include communications management for controlling and driving a network; applications processing of data in the network, including creating and managing data files; and multiple host access for terminals within the DSS domain.

A file-level host interface enables host application programs to use IBM 2400/3400 tape commands to

communicate with system resources. Basic message handling and queuing are supplied for data being transmitted through the network.

Also included are message switching by priority, network security, network statistics accumulation, and maintenance aids and services. The system can share a processor with the company's other software systems without affecting their independent operation.

Computer Peripherals

Release 2 of the software system supports various peripheral equipment which attach to the processors. Disc systems featuring the 7215 storage control unit have either fixed or removable media drives. Fixed drives have capacities of 24M (model 6124) or 48M bytes (6148); removable types feature 150M (6215) or 300M bytes (6230).

The 7322 combines a mag tape drive unit and controller in one cabinet, with capability to add up to three more drives (6322 mag tape units). The 7305 and 7306 card readers read standard 80-col cards at speeds up to 600 and 1000 cards/min, respectively. The last peripheral—the 7406 line printer—prints lines of up to 136 char at speeds up to 600 lines/min.

Shipments for the processor and DSS Release 1 are scheduled for the first quarter of 1978. DSS Release 2, along with the peripherals, is scheduled for the third quarter of 1978.

Circle 404 on Inquiry Card



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Now, you can order our DASHER™ terminals, even if you don't own a Data General computer system. Both our fast impact printer and our user-oriented video display are interface-compatible with any standard computer system.

60 or 30 cps versions of the DASHER printer, with a standard typewriter keyboard, u/l case, 132 columns.

DASHER display features a 1920 character screen, u/l case, detached keyboard, programmable function keys, and a monitor that tilts and swivels.

For more details call your Data General sales office or nearest independent supplier of Data General terminals. Or write. Even a bit of Data General in your computer system is better than none.

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Study Assesses Computers, Telecommunications, and Information Policies

At the request of the Congressional Office of Technology Assessment (OTA), the American Federation of Information Processing Societies, Inc. (AFIPS), 210 Summit Ave, Montvale, NJ 07645 is serving as a member of the OTA Telecommunications, Computers, and Information Policies Working Group together with "parties at interest" such as AT&T and IBM Corp; consultant firms including Rand Corp and Arthur D. Little, Inc; and selected executive agencies including the FCC and the White House Office of Telecommunications Policy. The working group is developing a framework for assessing various aspects of information technology.

At the first meeting on May 2 and 3, in Arlington, Va, Philip S. Nyborg, director of AFIPS' Washington office, presented for discussion a

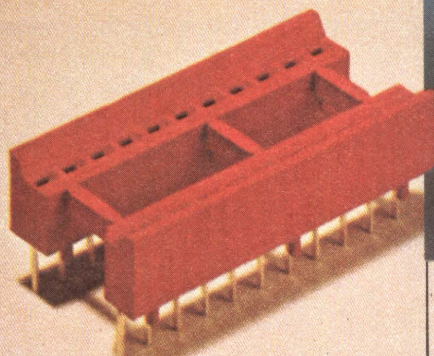
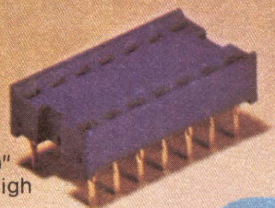
Whatever you need in an IC socket... **RN has 'em all!**

—and with “side wipe” reliability

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NEW! ICL Series

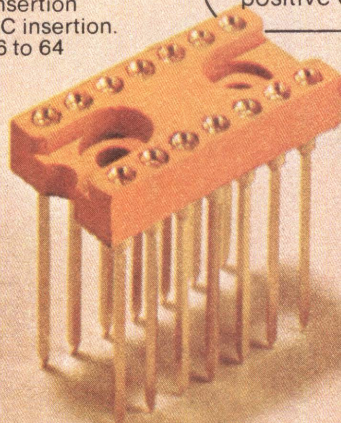
26% lower profile—.150" Ideal for high density, high volume configurations, provides maximum vibration resistance. Solder type, single leaf “side-wipe” contacts. 8 to 40 contacts.



ICN Series high reliability general-purpose sockets. Low insertion force allows automatic IC insertion. In solder or wire-wrap. 6 to 64 contacts. Dual leaf “side-wipe” contacts.

ICA Series

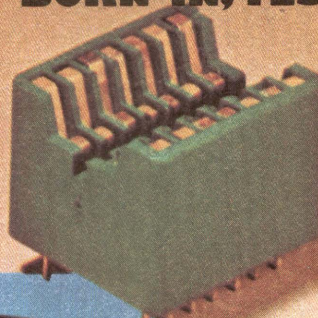
high reliability pin socket contacts. Low profile in solder or wire-wrap. 8 to 40 contacts.



BURN-IN, TEST SOCKETS

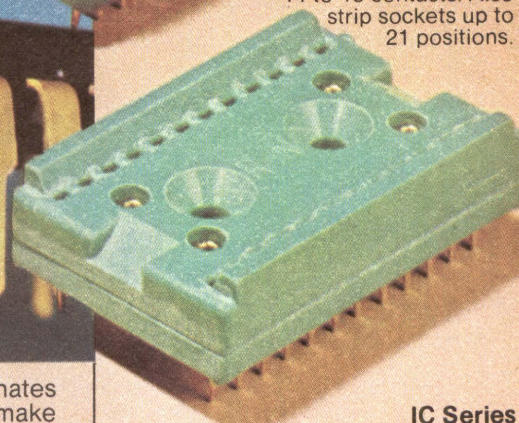
TS Series

very long contact life. Very low insertion force. Ideal for incoming inspection. With 14 to 40 contacts. Also strip sockets up to 21 positions.



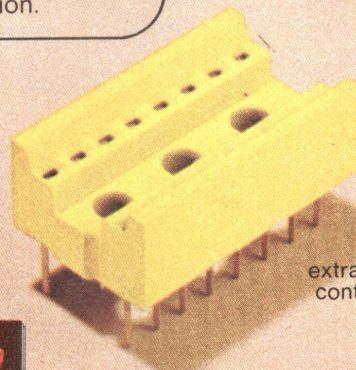
IC Series

moderate cost, long life. Designed for general test and burn-in up to 350°C. With 14 to 40 contacts.

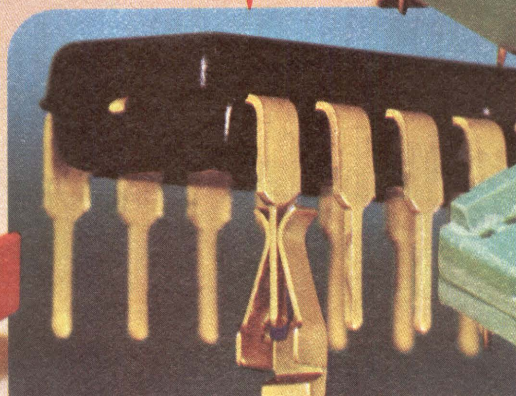


ICN/S2 Series

lowest cost burn-in socket available. Designed to accept IC extraction tool. With 8 to 40 contacts, with strip sockets up to 25 positions.



RN HIGH RELIABILITY eliminates trouble. “Side-wipe” contacts make 100% greater surface contact with the wide, flat sides of your IC leads for positive electrical connection.



WRITE TODAY
for New RN “Product Selection Guide”...



... and informative book “What to Look for in IC Interconnects.” Free from RN—the people who make more kinds of high reliability sockets than anyone.

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CIRCLE 19 ON INQUIRY CARD

You've already conceptualized and developed the software...

Introducing Tektronix' 8001 Microprocessor Lab: a total hardware debugging environment for the design of microprocessor-based products. Featuring multiple microprocessor support, in-prototype emulation, and real-time trace, the 8001 provides a comprehensive technique for exercising and debugging already developed software on your prototype.

In the tradition of the TEKTRONIX 8002, this new microprocessor design aid offers support for many types of microprocessors, including

the Intel 8080, Motorola 6800, Texas Instruments 9900, and Zilog Z-80. The 8001 can support both 8 and 16-bit microprocessors.

The Microprocessor Lab also offers three emulation modes for system-controlled, partial, and full emulation . . . on the same microprocessor you'll be using in the finished product. A memory mapping technique for gradually releasing program functions to the prototype and systematically isolating program errors. A real-time trace option which allows you to monitor microprocessor activity at full speed.

And one other key feature: the comprehensive service and support that only an instrument company can provide.

...now put it to the test in a total hardware debugging environment.

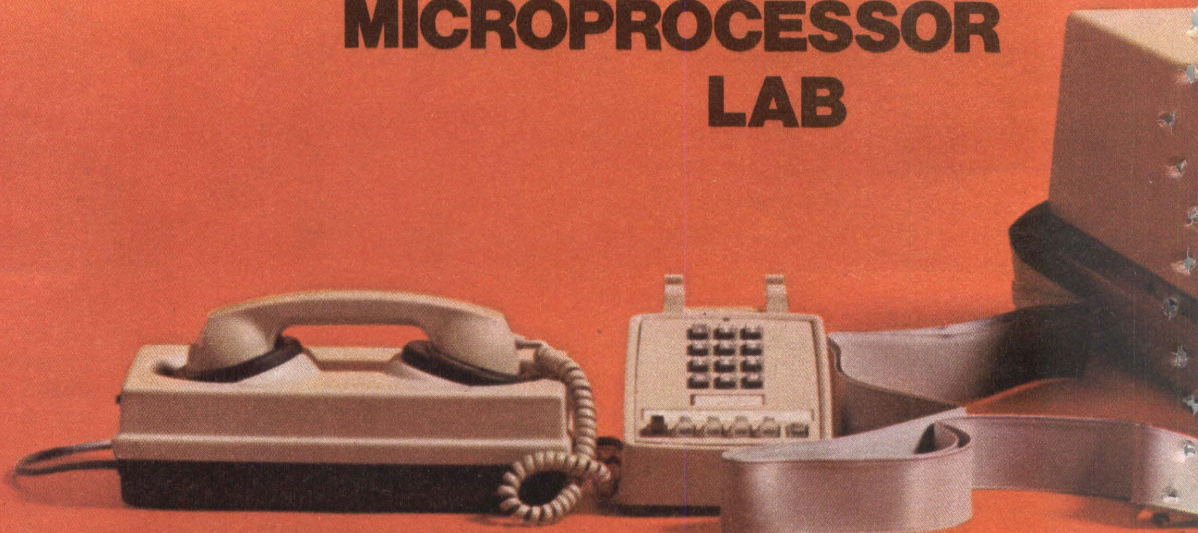
A Typical Development Sequence Using The 8001

The initial design cycle has been completed. Software and hardware functions have been assigned; prototype hardware has been built and preliminary debugging checks have been run using the 8001; software has been developed and partially debugged on an external software development system. The program is downloaded to the Microprocessor Lab through any RS-232-C compatible medium (such as modem or paper tape), and the critical integration phase begins.

The program is first tested in system-controlled emulation (mode 0) on the 8001 *emulator processor*. This "dry run" enables you to detect any software errors that may not have shown up at the assembly level.

In partial and full emulation (modes 1 and 2), the program is exercised on the prototype with the 8001 *prototype control probe* connected to the

THE TEKTRONIX 8001 MICROPROCESSOR LAB



emulator processor at one end and plugged into the empty microprocessor socket in prototype circuitry at the other. This lets you integrate in stages while you maintain control through the 8001.

In partial emulation, the program runs using 8001 memory space and prototype I/O and clock. With the memory mapping feature, memory may be mapped over to the prototype by address blocks. This enables you to localize program errors . . . or even "patch" around a faulty bit or routine. Throughout partial emulation, program activity may be accessed via the powerful 8001 *debugging system*, which allows you to trace, set breakpoints, examine and change memory and register contents.

In full emulation, the program is exercised on the now stand-alone prototype; you still maintain complete control through the Microprocessor Lab. All I/O and timing functions are directed by the prototype; all memory has been mapped over to the prototype; and only the prototype control probe is still in place, emulating the target microprocessor. Although the prototype is effectively freestanding, then, you still direct program activity, at the prototype end of the probe, from the 8001.

Real-Time Trace

With the optional *real time prototype analyzer*, you can dynamically monitor the prototype address bus, data bus, and up to eight other locations on the prototype circuit board. Prototype activity is monitored at full speed, without stopping or slowing up the working microprocessor. This enables you to locate critical timing problems and hardware/software sequence problems during partial and full emulation.

In this way, the 8001 provides a *total hardware debugging environment* supporting each successive phase of the product development cycle. After downloading object code, the designer proceeds from hardware test and software debugging, to the sequential integration of program and circuit, to final integration and test of the stand-alone product. The real-time prototype analyzer enhances partial and full emulation by allowing the user to monitor and access prototype activity in real time.

A Commitment To Microprocessor Design Aids

A growing product family . . . a full line of options and peripherals . . . a staff of highly trained microprocessor design aid Specialists and Field Engineers . . . a comprehensive service program . . . and years of experience in designing our own microprocessor-based products: all these things are a measure of Tektronix' commitment to the 8001 Microprocessor Lab.

For a demonstration of this innovative new product or for more information, write Tektronix, Inc., P.O. Box 500, Beaverton, Oregon 97077.

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For a demonstration, circle 21 on Inquiry Card.



statement of issues drawn from contributions of a special AFIPS panel representing its constituent societies. Intended to identify those issues which are appropriate for consideration, the statement includes 16 specific issues falling within seven basic areas: formulation of a coherent national information policy; nonregulatory approaches to implementing national information policy; coherent regulation of communications-related activities, in areas where there is a demonstrable need for regulation (possibly including electronic mail and EFTS); protecting individual rights; government actions for the "public good"; issues related to the Consumer Communications Reform Act; and significant technologies to be addressed in the OTA study.

Future meetings will be held to identify policy options and to define research strategy; specific assessments will be undertaken as requested by Congress and approved by OTA. It is anticipated that technology assessment may become a permanent OTA program, and may affect regulatory treatment of institutions offering computer communications services.

Sound Channel System Is Being Developed for Time Division Multiplexing

Offering up to five or 10 sound channels with a 15- or 7-kHz bandwidth, respectively, in a 2048k-bit/s channel, the PCM sound channel system will be available from Siemens Aktiengesellschaft, D-8000 München 1, Postfach 103, Germany at the end of the 1970s. The 15-kHz channels

are suitable for TV sound and mono and stereo sound program transmission and distribution via long-range paths, as well as program transmission to and from studios and to VHF transmitters. The 7-kHz channels are adequate for broadcasts and program transmissions to short-, medium-, and long-wave radio transmitters. They also permit combined transmission of sound programs, telephone calls, and data.

Order Is Sought In Planning of Communications Facilities

Reaffirming the need to return planning and negotiating functions to international telecommunications carriers, George F. Knapp, president of ITT World Communications Inc, 67 Broad St, New York, NY 10004 appeared before the Communications Subcommittee of the Senate Com-

merce, Science, and Transportation Committee to urge reemphasis of the FCC's role as the sole regulatory agency for communications. These changes would "bring order out of the present chaotic involvement of various U.S. agencies in the planning of international (communications) facilities," as well as "minimize duplication of effort and red tape involved in approval of overseas transmission facilities while maintaining proper regulatory supervision by the government." □

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Strength for today and precision for tomorrow. You buy both with the 4900 Slide. It's a full extension, complete ball bearing action slide which operates at a low noise level. Load capacity is 100 lbs. per pair. Space requirements are just 1/2" at each side and 1 7/8" height. (All this at an unbeatable price!)

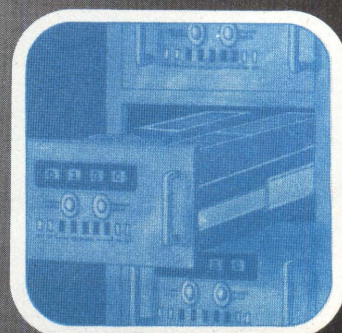
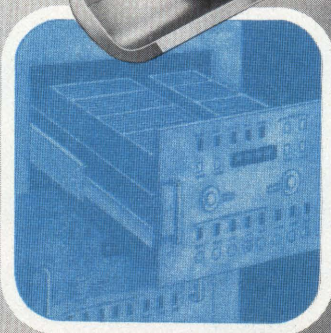
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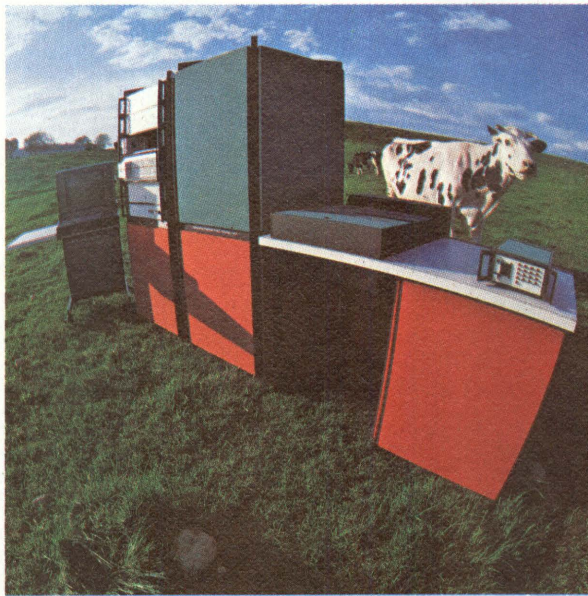
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Quite frankly, we're going to be #1 in memory testing till the cows come home.



Four years of matching the memory industry breakthrough for breakthrough have made Teradyne the leader in memory testing.

We started back in 1973 with the J384, a dedicated memory test system. It tested RAMs and ROMs efficiently and economically. But things were changing fast.

1974 saw the advent of dynamic devices like the 4k 2107. And we added the M385 microprogrammable pattern

generator to keep pace.

In 1975 our answer to increasingly complex memory technology was a new system, the J387.

In 1976, when 16k and page-mode parts went into production, we responded with the H712 test deck.

Today, Teradyne has an installed base of well over 100 J380-series memory test systems working for more than

20 companies. At probe, at final test, and at incoming inspection. That's a larger dollar base than our two nearest competitors combined.

Four years of experience have made us the most capable source of memory test equipment in the world.

If you test semiconductor memories, call us today. You'll call us eventually. Because no matter where memory technology goes from here, Teradyne will be there.

TERADYNE

Semiconductor Test Division
Boston, Mass. - Chatsworth, Calif.

High Performance CPU and 64k Memory Packed Into Desktop Computer

System 45 integrates central processor, mass storage, typewriter keyboard, standard language, convenient tape media for data or program input, and an alphanumeric and graphics CRT in a desktop system. Designed by Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304 to make maximum use of each component's performance, the system closes the gap between console-based minicomputers and desktop calculating systems—offering the power of the first and the size and ease of use of the latter.

The system's BASIC interpretive language conforms to the ANSI standard for minimal BASIC, allowing existing software to operate directly. In addition, it provides subprograms, multi-character identifiers, line labels, powerful array operations, and flexible output formatting. To simplify use of the enhanced language, the standard keyboard has separate groupings of keys for program control and editing, CRT control, and 32 user-definable functions.



Hewlett-Packard's System 45 integrates keyboard, CPU, 64k main memory, 12" CRT, and tape input/storage media in compact computer that is based on BASIC language to provide rapid solutions for user problems

Users can access 13,498 bytes of the 16k bytes of basic read/write memory; when expanded to 64k bytes (in 16k increments), 62,650 bytes are user-accessible. 98k bytes of ROM

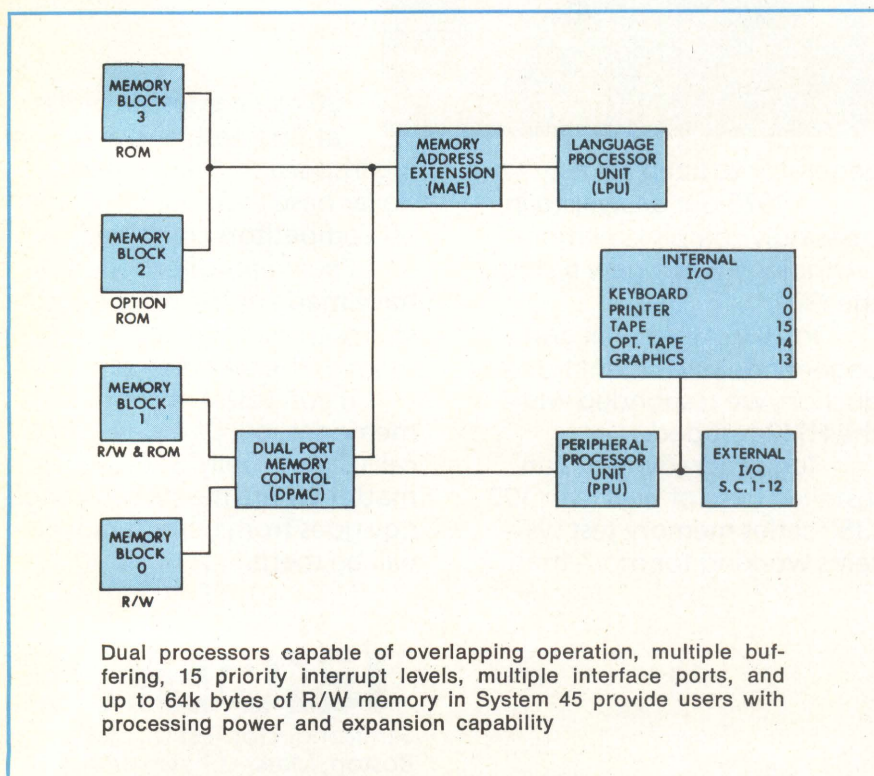
store the operating system, including drivers and utilities. Plug-in ROM packages provide additional optional capabilities such as graphics.

Two processors are controlled by the ROM operating system controls (see diagram). The peripheral processor unit (PPU) executes the operating system contained in block 1 ROM, coordinating the two processors and all I/O transfers. The language processor unit (LPU) controls program execution by executing instructions in block 3 ROM, block 2 option ROM, or block 0 R/W, in the case of binary programs. Processor communication is via shared R/W memory. Block 0 R/W memory is used to store users' program, data, user-definable key definitions, dynamic I/O buffers, and some system R/W.

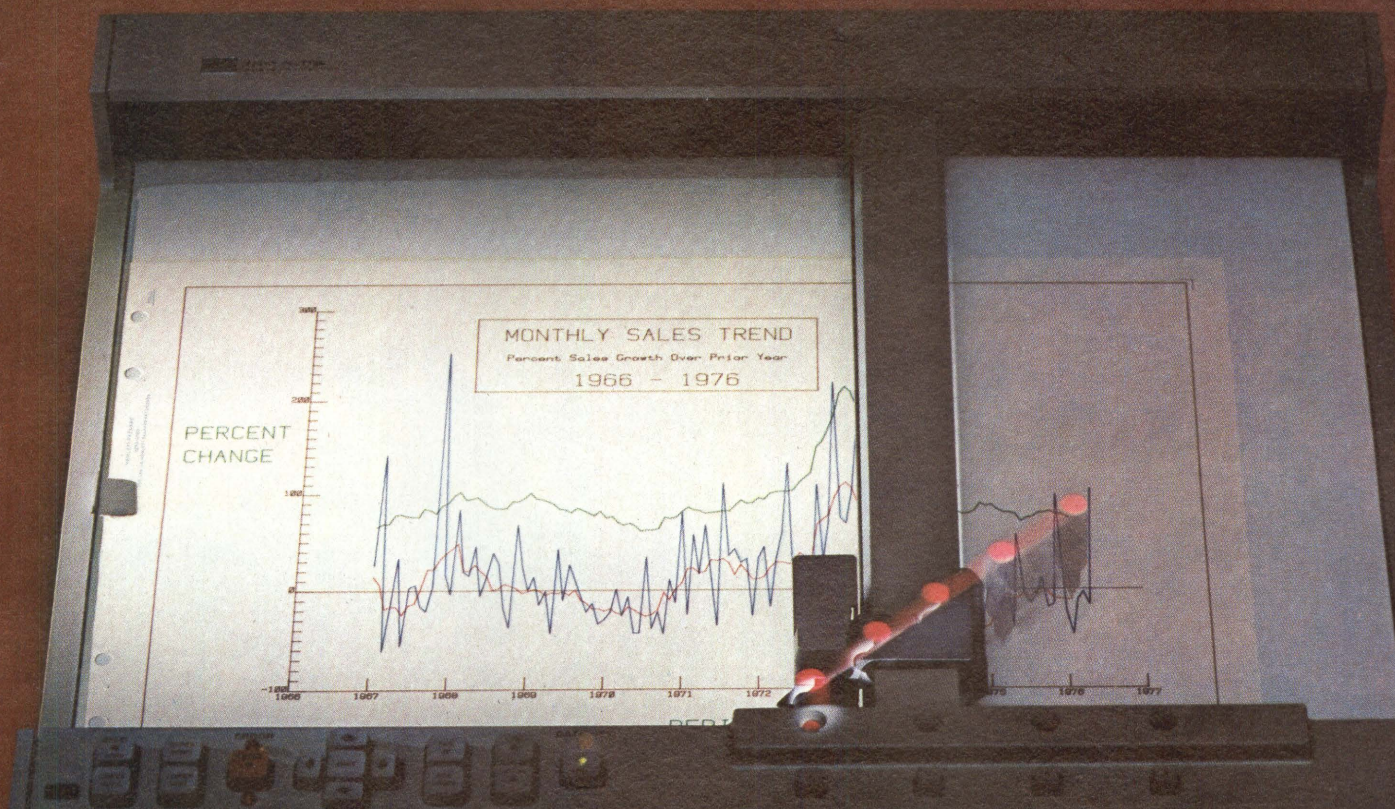
Use of dual processors offers several methods of providing greater throughput of I/O operations. The PPU performs actual transfers to the I/O devices, while the LPU executes the program. Dynamic buffering allows the LPU to complete its part of the I/O statement execution as quickly as possible. I/O operations are automatically overlapped with each other using interrupt and DMA control.

Overlapping of I/O operations is invoked by executing the overlap statement either in the program or directly from the keyboard. While in overlap mode, the LPU initiates I/O operations when it encounters them in the program, and continues executing the program. The PPU logs the I/O operations on a queue associated with the device, then continuously examines the operation at the head of each queue and attempts to advance it to completion. When actual transfer of data from a device is initiated, the PPU is free to execute another I/O operation, with the transfer occurring in a background interrupt service routine. When transfer is complete, the operation is removed from the queue.

Overlap mode can increase program execution speed by a factor of nearly $N + 1$ where N is the number of I/O devices concurrently active. This ideal maximum speed would occur only when all overlapped operations are of equal time duration and the program is structured properly. Although this ideal is impossible to attain, significant increases in program execution speed can be obtained by invoking overlap mode.



In only 90 seconds of transmission time, HP's new graphic plotter drew this chart in four colors,



picked up its pens, and put them away.

Neat, isn't it.

Getting this kind of graphics from complex computer data has always been a long drawn-out problem. Now, arcs, circles, dashes, dots, and alphanumeric—routine shapes that normally take lengthy programs—are quickly drawn by single commands.

And, with only one transmission, any series of shapes and moves can be stored in the plotter's memory and repeatedly executed as macroinstructions.

But the neat trick is the way our plotter instantly changes colors via a program-

mable command or front panel control. Four long-life HP pens stay tucked away until the plotter picks one out, draws, and puts it back (with the cap on).

You have to see it to believe it. HP's remarkable new Model 7221A (RS 232C interface) uses an internal memory and 40 commands that plot efficiently to save you money in computer and transmission time. All for just \$4,600, domestic USA price only.

See your Hewlett-Packard representative for complete details on how you can have eco-

nomical high quality multi-color charts and diagrams of your computer-generated information with the new Model 7221A Graphic Plotter. It's the neat solution to the problem of long, drawn-out hard copy graphic displays. 11712

CIRCLE 24 ON INQUIRY CARD

HEWLETT  PACKARD

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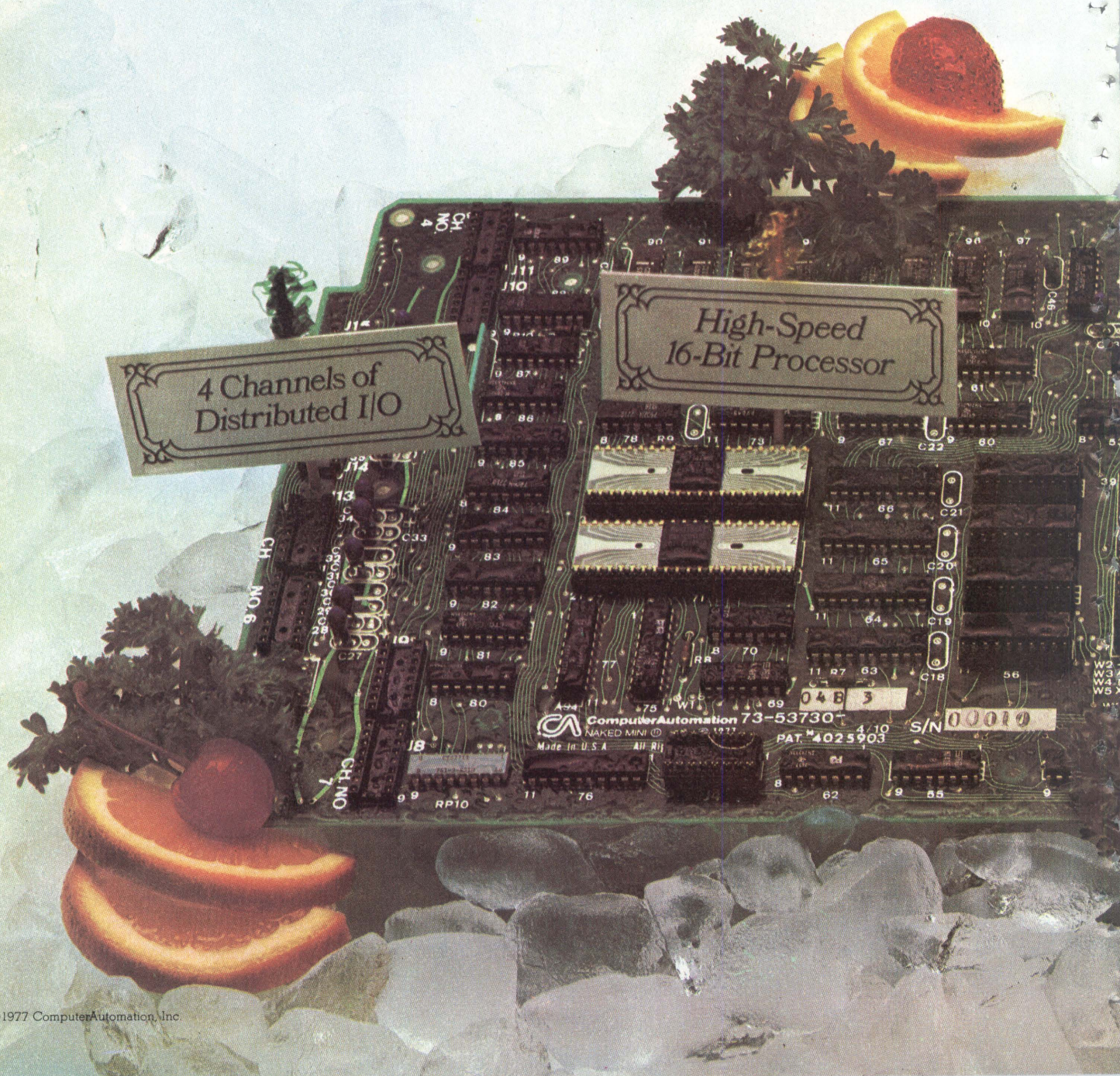
For assistance call: Washington (301) 948-6370, Chicago (312) 255-9800, Atlanta (404) 955-1500, Los Angeles (213) 877-1282

ComputerAutomation's NAKED MINI® 4/10 is the most exciting spread we've ever dished up: a high-speed, versatile, 16-bit processor, up to 4K words of RAM/PROM memory, and four distributed I/O channels. All on a single board. And this powerful, multi-register minicomputer sells for micro prices.

Value, however, is a lot of things. Such as performance, versatility, and a faster, lower cost way of getting a product to market. For the 4/10, your real savings just begin to start with the sale price. Its large instruction set (including multiply/divide as standard) pays off with exceptional programming versatility, faster development, less memory used. Options include floating-point instructions and double-register shifts.

Its four distributed I/O channels are another money saver, cutting interfacing costs by up to half. Our unique Intelligent Cables (19 available) give you interface capability with a broad variety of standard and nonstandard peripheral devices. Distributed I/O has other advantages. Its auto I/O instructions are easier to program, take less memory, and execute faster than traditional programmed I/O. And it has the advantages of DMA at about half the cost.

SMORGA



The 4/10 has 64K-word addressing and a MAXI-BUS that allows interfacing with the wide variety of interchangeable memories and I/O controllers in the NAKED MINI 4 family.

What about software? It's one of the 4/10's real strengths. Not only a wide range of software, but also software optimized individually for both development and execution needs.

Available software ranges from the simplest—a memory-based system that runs in as few as 4K

words—through the most sophisticated, a full-blown, disk operating system that supports FORTRAN IV, BASIC, PASCAL, and MACRO 4 assembler.

In terms of hardware and software, the 4/10 is fully compatible with its higher performance brothers, the 4/30 and 4/90.

Okay, we've served up our new 4/10 mini with lots of standard and optional hors d'oeuvres. Still hungry for information? Contact Department 1161, NAKED MINI Division, 18651 Von Karman, Irvine, CA 92713, (714) 833-8830, for our new brochure. It's quite a bit of food for thought.

SBOARD.



ComputerAutomation

Naked Mini. Division

CIRCLE 25 ON INQUIRY CARD

4K RAM Memory

LSI 4/10
\$645
LIST PRICE

NAKED MINI products are sold only under volume purchase agreements.

Other system features include the 12" CRT which provides a 560 x 455 dot matrix in graphics mode and a full 80-char wide, 24-line display in alphanumeric mode. Available as an option is a built-in thermal line printer which will produce 80-char lines at 480/min, and is capable of transferring graphical images from the CRT in seconds.

Storage for data and programs is provided by a built-in 210k-byte tape cartridge system (a second is optional), an external 460k-byte flexible disc drive, or external hard disc drives with capacities of 15M to 50M bytes. Commands are device-independent, permitting access to any of these devices by simply changing the address of the device.

Multiple interface ports and capability to use bit-serial, BCD, bit-parallel, and HP-IB interfaces allow users to expand the system. Its four I/O ports hold a range of interface cards which enable the system to accommodate multiple hard discs or to acquire data from as many as 20 instruments.

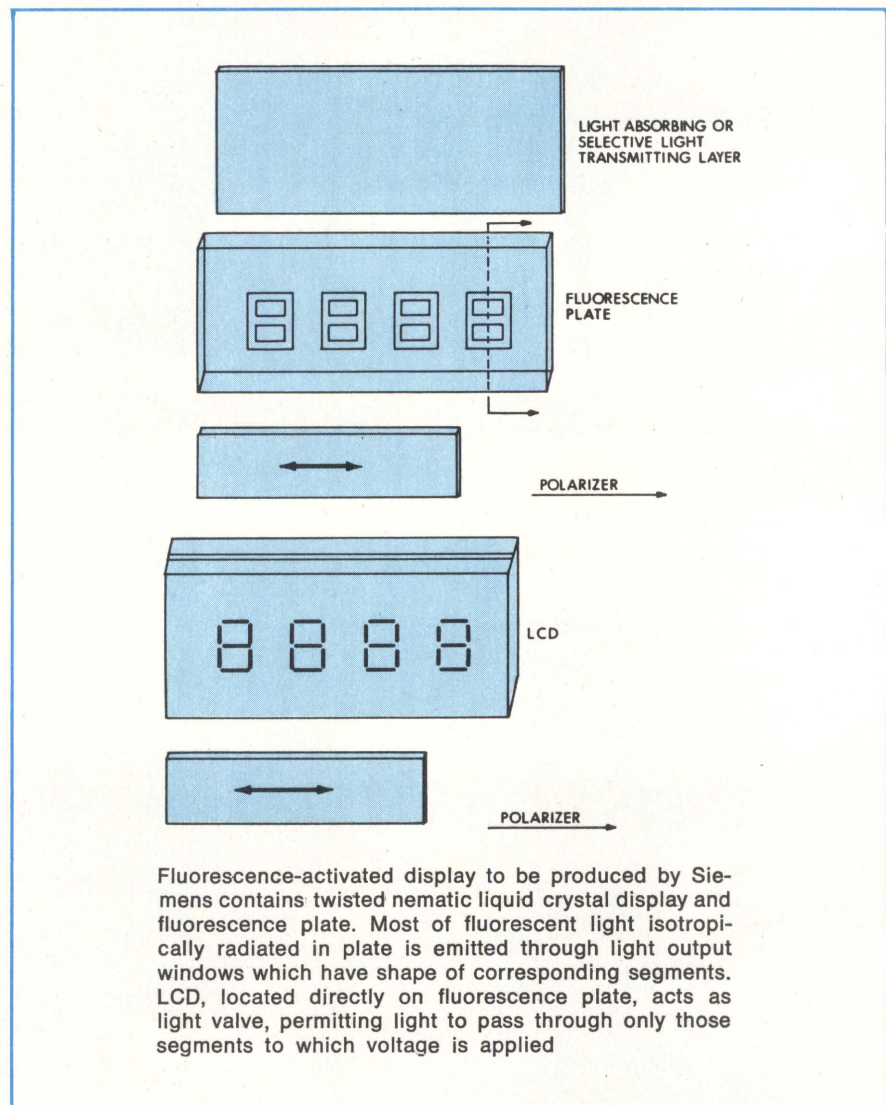
The compact, 18.5 x 19 x 26.5" (47 x 48 x 67.3 cm) package weighs 75 lb (34 kg), allowing its use where portability is required. Complete with keyboard, 16k memory, CRT, and one tape transport the unit is priced at approximately \$12,000.

Circle 140 on Inquiry Card

Fluorescence Activated LCDs May Serve In Low Light Conditions

A fluorescence-activated liquid crystal display (LCD) with luminosity comparable to that of light-emitting diode (LED) displays provides red, green, and orange color effects and overcomes some disadvantages associated with passive displays. The fluorescence-activated displays collect the ambient light, focus it toward the segments of the display, and greatly amplify the display's brightness, thus increasing the application range of LCDs.

Principle structure of the fluorescence-activated display (see diagram) consists of an LCD and fluorescence plate. The fluorescence plate consists of plexiglass in which fluorescent molecules are dissolved. The small sides of the plate are coated with a highly reflective material. The plate has mirror coated grooves on



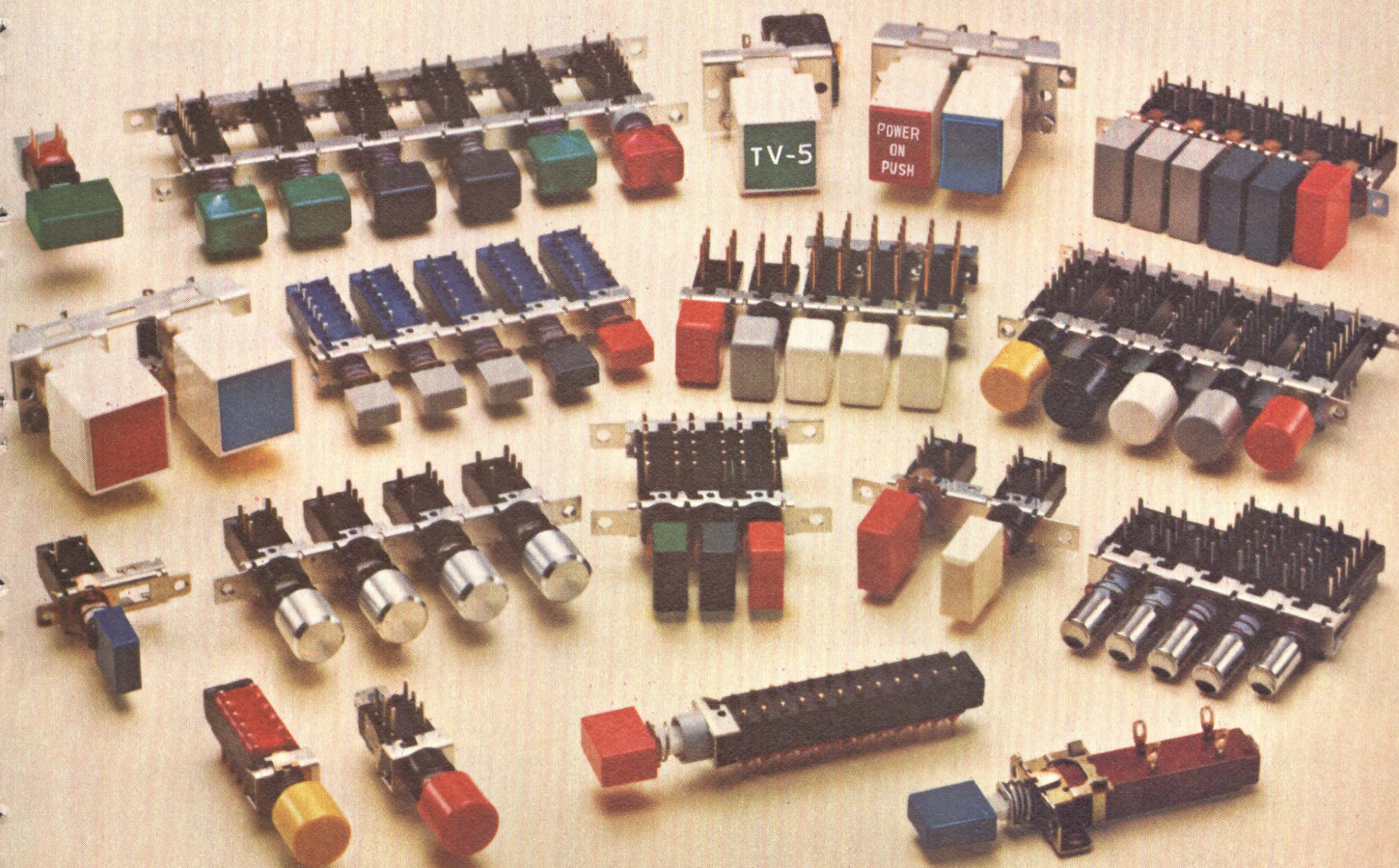
its back and light scattering areas on its corresponding front side. This arrangement allows fluorescent light produced in the interior of the plate to leave the plate only within a certain angle. In the case of plexiglass, this means about 24% of the total; the 76% remaining in the plate can leave only through the "output windows." To obtain a high radiance of segments, a large area fluorescence plate is used. Area of digit segments is based on the desired digit size.

Fluorescence efficiency depends on emission and absorption characteristics of the fluorescent materials embedded in the fluorescence plate. With the display material available until now, the emission band and the absorption band of the dye stuff have overlapped, weakening the intensity of the emitted fluorescence light by

self-absorption. While the synthesis of red, orange, and green fluorescent dyes with very low self-absorption is now possible, it remains a challenge, since concentration of fluorescent materials must be determined so as to absorb environmental light almost completely at a single or double pass of light through the plate. Only twisted nematic cells are used for LCDs. The twist cell consists essentially of two glass plates with transparent electrodes in the shape of the characters to be displayed; in between these is a liquid crystal layer of approximately 10 μm .

Without electric field, the liquid crystal molecules are mostly aligned in the plane of the electrodes. At its feedthrough, the plane-polarized light wave is rotated by about 90 degrees. Polarizer foils, applied

Who offers more pushbutton switch options to meet your design needs? . . .



CENTRALAB!

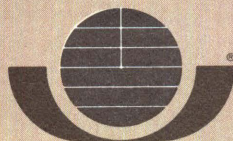
Why restrict your switching designs to a few limited options? Come to Centralab . . . The pushbutton switch manufacturer that offers you true design flexibility.

Shown above are 18 of the most popular options available. They're described at the right. Included are *epoxy sealed terminals with built-in standoffs at no additional cost. And more programming capabilities using lockout options than any other supplier.* With a wide choice of lighted and non-lighted buttons.

There's one feature of Centralab pushbutton switches that's not an option. *It's Centralab Service.* It comes with every switch. Proof? We'll send you samples with your choice of options in one week . . . Production quantities in six.

For a complete catalog of Centralab pushbutton switches, options and prices, talk to your Centralab Technical Representative, or call (515) 955-8534.

*Products you need
from people who care.*



CENTRALAB

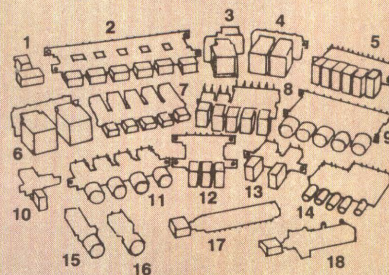
Electronics Division

GLOBE-UNION INC.

P.O. BOX 858

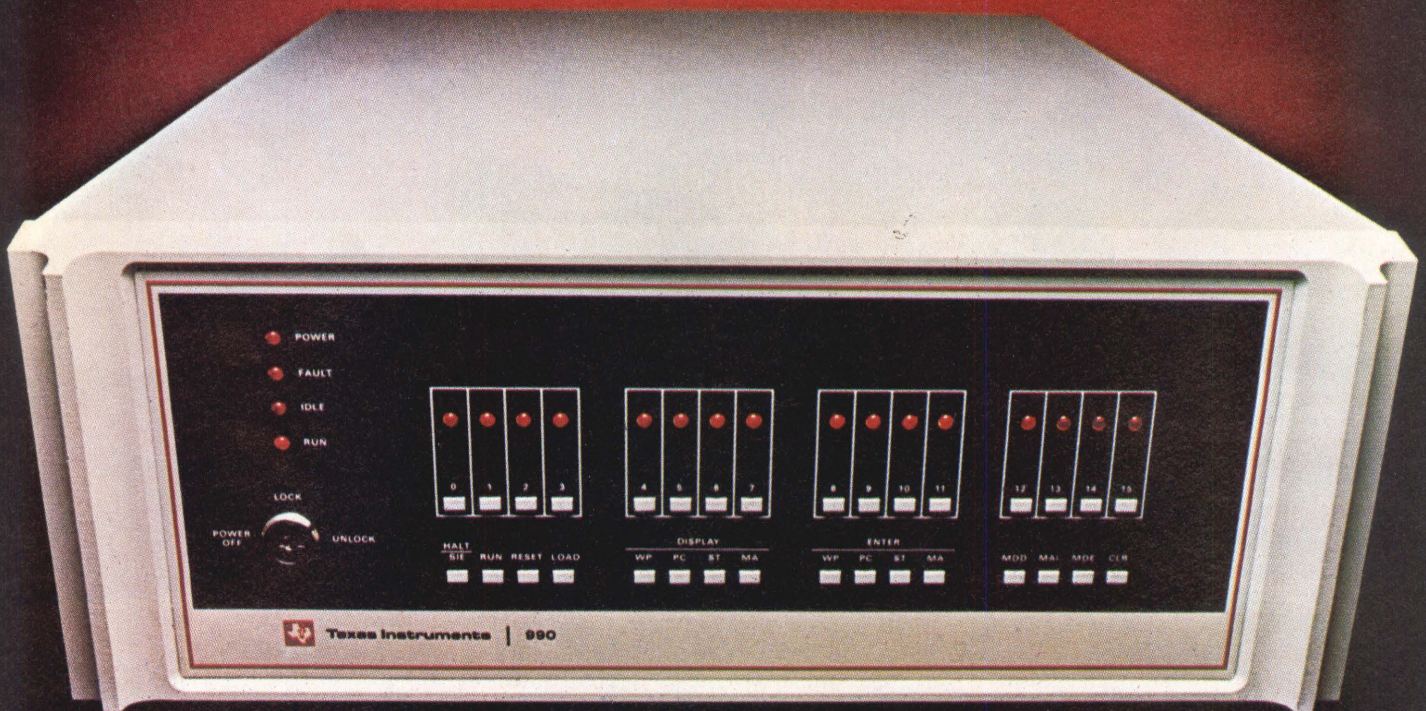
FORT DODGE, IOWA 50501

Key to Picture Above



- | | |
|---|---------------------------------------|
| 1. Dust seal cover. | 9. Master-on lockout. |
| 2. Interlocking lockout. | 10. Selective pin cutting. |
| 3. Lighted TV-5 line switch. | 11. Momentary actuation. |
| 4. 17.5 mm lighted switch with flat and concave lenses. | 12. Momentary lockout. |
| 5. Panel offset bracket. | 13. Push-push and momentary assembly. |
| 6. 20 mm lighted switch with recessed lenses. | 14. Override cam release function. |
| 7. Dialyl phthalate insulation. | 15. Epoxy seal. |
| 8. 10 mm gold terminals. | 16. Rear coupler. |
| | 17. Terminals with built-in standoff. |
| | 18. 2 amp. line switch. |

990 OEM minicomputers.



**Built, backed and priced
to sharpen your competitive edge.**

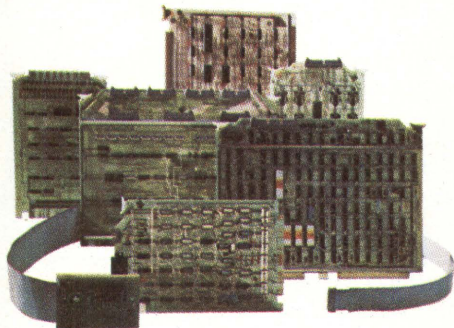
TEXAS INSTRUMENTS.

The 990/10 minicomputer from TI brings superior value to both you and your customers.

Starting with field-proven hardware, the 990/10 delivers the reliability you expect from TI. And all the off-the-shelf support you need for user applications. You get standard software languages, a broad choice of peripherals and nationwide service.

Built for more processing power.

The 990/10 is the most powerful member of the 990 computer family. Its architecture provides features that give you maximum processing power for your money. Like hardware multiply and divide. A 16-level hardware



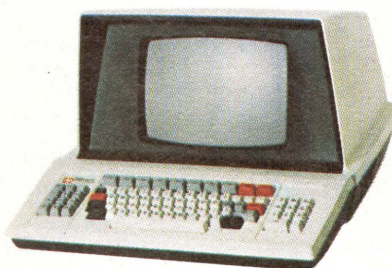
Peripheral Interface Modules

interrupt structure. 16 registers arranged in a workspace concept. I/O that's directly programmable through the Communications Register Unit (CRU) and autonomously through a high-speed data bus. And bit, byte and word addressing of memory.

Built for system flexibility.

In small or large configurations, the 990/10 design provides surprising flexibility for a small investment.

The CRU, with up to 4096 I/O lines, reduces interfacing costs by keeping controller complexity to a minimum. The TILINE* asynchronous high-



Model 911 Video Display Terminal

speed data bus can support both high- and low-speed devices and takes advantage of design simplicity for simultaneous data transfer between peripherals, the CPU and memory.

With the 990/10, you get a powerful instruction set with an extended operating feature that allows hardware to take over operations that software would normally execute. An optional mapping feature provides memory protection and memory expansion to 2 million bytes. And, optional error-correcting memory corrects single-bit errors for increased system reliability.



*DS 25/50
Disc Drives*

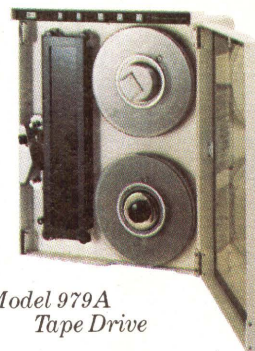
Full peripheral support.

As well as a range of standard peripherals, disk storage to 180 million bytes and magnetic tape with 800 and 1600 bpi options are available for low-cost mass storage and back-up.

A choice of software.

With common higher level languages, FORTRAN IV, COBOL and Multiuser BASIC, plus the 990/10 assembly language, you have all the tools you need for an efficient application program.

Both the disk-based and memory resident operating systems give you modularity and flexibility for system generation to meet application de-



*Model 979A
Tape Drive*

mands. We offer program development aids for creating and testing software, and communications software to support synchronous or asynchronous data transmission.

Backed with nationwide service.

Our responsibility to you doesn't end with the sale. We follow through with complete system training, plus a nationwide factory service network.

The TI 990/10 minicomputer. We build it, back it and price it the way you and your customers want it. You can start configuring a system now with our 990 Computer Systems Handbook on the upward-compatible family of the TMS 9900 microprocessor, 990/4 microcomputer and 990/10 minicomputer. For your free copy, send a letterhead request to Texas Instruments Incorporated, P.O. Box 1444, M/S 784, Houston, Texas 77001.



TEXAS INSTRUMENTS
INCORPORATED

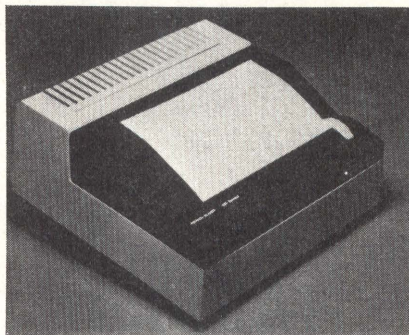
plane parallel onto the glass, do not allow light coming from the fluorescence plate to pass. When a voltage of approximately 3 to 9 V is applied, the polar molecules rotate and align themselves along the field lines perpendicular to the glass surface, the 90-degree rotation of the light vector is eliminated, and light is transmitted through the liquid crystal cell. Thus, the segments radiate brightly.

Display numbers are seen bright on a dark background. Brightness of the display adapts automatically to surrounding brightness. Radiant intensity of the digits equals the product of fluorescence efficiency times the light collection factor, which is equal to the ratio of the fluorescence plate surface to the surface of the segments.

Developed by the Institute of Applied Solid State Physics, the display will be produced by Siemens Aktiengesellschaft, München 1, Postfach 103, W Germany, during 1978. Circle 141 on Inquiry Card

Thermal Printer Provides Hardcopy at 100 Char/s from CRTs

A quiet printer with only one moving part, the model 650 CRT page printer



Rated at 100 char/s, Perkin-Elmer's fully buffered model 650 is capable of printing full CRT screen in 20 s, while terminal concurrently processes data or communicates with host computer

is capable of printing full 1920 character screens from any CRT terminal in less than 20 s. The fully buffered, microprocessor-controlled thermal printer—introduced as the Pussycat by Perkin-Elmer Data Systems, Terminals Div, Rt 10 and Emery Ave, Randolph, NJ 07801—accepts data as fast as it can be transferred from any CRT having the RS-232 interface.

Producing a full page pattern with a resolution of 288 x 720 dots/page, the unit uses standard letter size paper impregnated with a colorless, heat-sensitive dye. Printing occurs as selected dots on the fixed head are

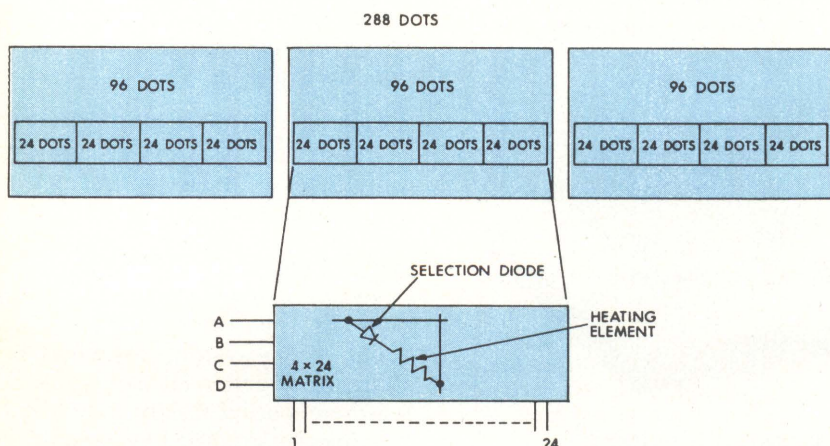
heated, causing the dye to change color. The soft platen paper transport—the terminal's only moving part—serves as print surface as well as transport. Printing heads consist of thick film thermal dot arrays and are fixed in position. Heating of the dots is controlled by the unit's Motorola 6800 microprocessor.

While the technologies employed in developing the unit are existing ones, their applications are novel. The dot matrix printing heads, for example, print sideways to reduce electronic components and associated costs. This is achieved by the microprocessor's character generator. Using the microprocessor to control the slew increases print speed; its control of the thermal printing reduces size of the necessary power supply.

Long wait times associated with line printers are eliminated by providing a buffer capable of storing the full contents of the 1920-char CRT screen. Data for an entire page are transferred to the buffer in just 2 s, providing minimal interruption of operator activity. By having the 288 printing elements scan horizontally—move the paper horizontally, and print by column, from left to right—the most effective means of printing is achieved.

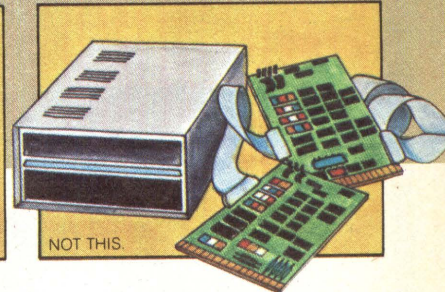
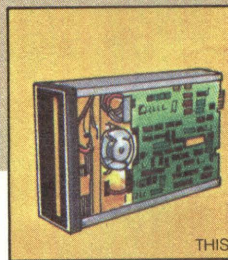
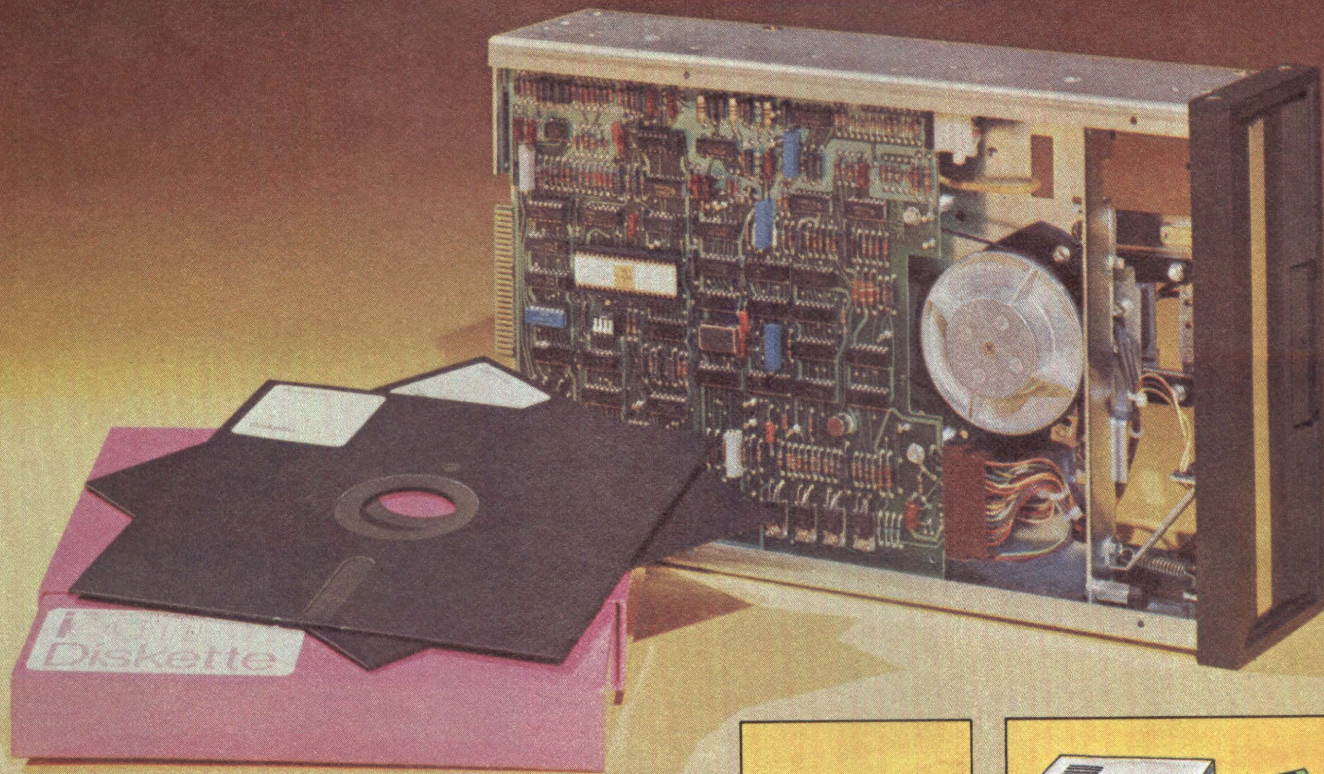
Data are stored in the printer's buffer, in a horizontal pattern as they appeared on the screen. The microprocessor scans the data vertically, picking up the first character on each line. At the same time, via a character generator which is part of the control program, it selects the dot pattern that corresponds to the first of the nine lines of dots that make up the first column of characters. This information is loaded into the 72-bit shift register, and the matrix input to the thermal head is turned on for 5 ms. Each column of dots is printed in four shots to reduce the amount of power needed.

The 3-part thermal printhead has a total of 288 active thermal elements along the top. Each separate head is supported on a flexure hinge to ensure good contact between the reactive dots and paper. Operationally, the 288 elements are considered as one head; however, there are actually three heads, each with four sets of 24 heating pads or dots. A multiplexing arrangement is used to fire the dots, reducing the amount of power and the cost of electronic parts.



Printing heads in model 650 consist of three thick-film arrays, each with four sets of 24 heating pads. Multiplexing arrangement is used to fire dots for each column in four shots, reducing amount of power required as well as cutting number of electronic components needed

iCOM's Intelligent Floppy.™



Controller/Formatter built-in. Packaging problems designed out.

When designing a floppy disk into a compact microcomputer-based system, engineers have been plagued with the problem of where to mount the controller/formatter cards and associated cables.

Our new FD5200 Intelligent Floppy™ solves this packaging dilemma by mounting all circuitry, including the single chip LSI controller/formatter, as an integral part of the disk drive chassis. A neat idea!

The 8 bit bi-directional bus makes it simple to integrate the iCOM® FD5200 into any system. Accrued benefits include: reduced hardware costs, smaller size, shorter assembly time, easier software development, improved reliability and lower maintenance. A mighty impressive list!

Compatibility to IBM 3740 Format... and Others

The special LSI controller/formatter chip provides the complex logic needed to write data on the diskette in IBM 3740 format — or other user selected formats as well. Another big plus is a phase-locked-loop for data and clock bit separation, and address word detection, which maximizes data reliability.

Pertec Makes the Driving Easy...

Since a floppy disk drive system is only as good as the mechanics, we use our field proven Pertec drive with three step-per-track head positioning for better accuracy and the unique head retract system for longer media life.

Why iCOM®?

iCOM® part of Pertec Computer Corporation, is one of the world's largest manufacturers of Microperipherals®. Thousands of our floppy disk systems are operating reliably in the field. And many major computer manufacturers have incorporated iCOM® floppies into their systems. Which means we deliver — and will be around to give you service whenever and wherever you may need it.

Speaking of Delivery... and Price

Our new FD5200 Intelligent Floppy™ is available now at a unit price of just \$795. Naturally, OEM discounts are available.

So phone us today. Or send for our brochure.

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CIRCLE 28 ON INQUIRY CARD

CENTRAL INTELLIGENCE:



The data formatter that came in out of the cold.

Tape drive intelligence has crossed the iron walls. And taken up residence *inside* a broad series of transports—through a special Microformatter™ that Pertec installs internally.

A real technology breakthrough for sure. But it's the hot savings potential that intrigues OEMs most.

Eliminates the need for any external formatter to control the reading and writing of data. Makes interface chores much easier.

Now add in the convenience and cost-efficiencies you'll realize with just one system to handle (and ship), instead of two separate devices.

Saves integration time. With the Microformatter built-in, a single interface can be used for 800 cpi NRZI, 1600 cpi PE, or dual formats.

Saves redesign. Formatted Tape Transports use the same Pertec industry-standard formatter interface. And the same Microformatter, to maintain parts commonality.

Saves daisy-chain hassles. Every master Formatted Transport can daisy-chain up to 3 more tape drives—either Pertec standards or our new Formatted models.

Saves rack costs. You free up former external-mount slots. And the single-board LSI

Microformatter is so compact it fits into each drive without restructuring standard rack mounts.

Internal Formatting. Deep down inside, you know it's right! And it's available in a flexible configuration range.

Formatted tension-arm: *FT7000*—compact 7" reel, NRZI or PE, 12.5 to 25 ips. *FT8000*—10½" reel; NRZI, PE, or dual NRZI/PE to 45 ips.

Formatted vacuum-column: *FT9000*—10½" reel, 37.5 to 75 ips NRZI, PE or dual. And *FT1000*—10½" reel, our vacuum column 125 ips high speed auto-thread, auto-load series, dual NRZI/PE.

Fully proven product. All are microformatted extensions of field-proven drives, produced by the world's largest independent manufacturer of peripheral equipment.

And backed by international sales/service facilities, with a long-term commitment to responsiveness. Making emergency assistance available on a 24-hour, 7-day basis, accessed through our toll-free 800 line.

At every level—product, sales, maintenance—Pertec intelligence has always recognized that cost-effectiveness is the central issue with OEMs.

- ☐ Please send full details on the Pertec Formatted Tape Transport Series.
☐ Send pricing information as indicated on the RFQ below (no obligation or cost).

Request for Quote

Formatted Series #	Reel Size	Tape Velocity (ips)	Recording Mode	Quantity Required	Date Wanted	Send Specs
FT7000	7"	12.5-25	PE or NRZI			
FT8000	10½"	12.5-45	PE, NRZI, Dual			
FT9000 Vacuum Column	10½"	37.5-75	PE, NRZI, Dual			
FT1000 Vacuum Column	10½"	75-125	Dual NRZI/PE			

Name _____

Title _____ Phone _____ Ext _____

Please attach coupon/RFQ to company letterhead and return to Pertec, 9600 Irondale Avenue, Chatsworth, CA 91311.

For immediate requirements, call your nearest Pertec regional sales office: Los Angeles (213) 996-1333. Ann Arbor, Michigan (313) 668-7980. Hudson, New Hampshire (603) 883-2100. England (Reading) 582115.

PCC PERTEC

a division of Pertec Computer Corporation

CIRCLE 29 ON INQUIRY CARD

Through firmware changes, the printer is capable of producing whatever is wanted. It can print any type of font within the 7 x 11 matrix. Even alphabets requiring proportioned spacing, such as Farsi, can be produced by using a programmable character set. By changing data stored in the character generator, the full 288 x 720 matrix can be manipulated, enabling graphics to be produced.

The unit has switch-selectable baud rates up to 9600. Mounted in a 4 x 12 x 12" (10 x 30 x 30 cm) case, it weighs 15 lb (6.8 kg). Price for the unit, with self-contained power supply, is \$795 in quantities of 75. Circle 142 on Inquiry Card

CMOS-Compatible Power FETs Switch Faster Than Bipolar

A significant development in discrete power semiconductors, VMOS power FETs from Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054 combine the best features of power transistors, SCRs, FETs, and vacuum tubes, providing an indestructible, CMOS logic compatible, high frequency device. Made using the VMOS (vertical MOS) process, VNXXAE series transistors can be used to replace power bipolar or Darlington transistors.

Because the technology produces devices with very high input impedance and low threshold voltage, it interfaces directly with TTL, DTL,

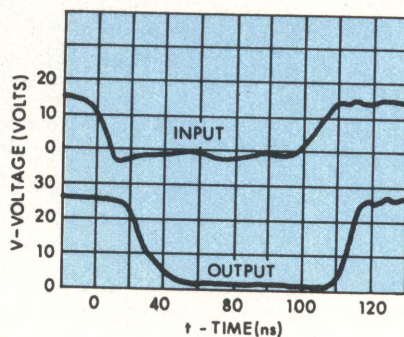
CMOS, and MOS logic families. Typical input leakage is less than 10 nA, allowing a fanout of more than 100 from CMOS. Built using a vertical, as opposed to a planar, technology, the FETs attain far greater density and provide ability to control greater current with the same input power.

The technology has a vertical rather than horizontal current flow, and provides current densities five to ten times higher than conventional MOSFET structures. The chip is diffused vertically, like a bipolar transistor, but has a MOS gate fabricated in a V-groove etched through the transistor body (channel region). This vertical processing results in a very short channel length. Current handling capability is inversely proportional to channel length and, therefore, the shorter channel contributes to increased current density.

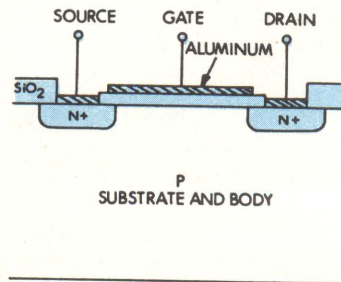
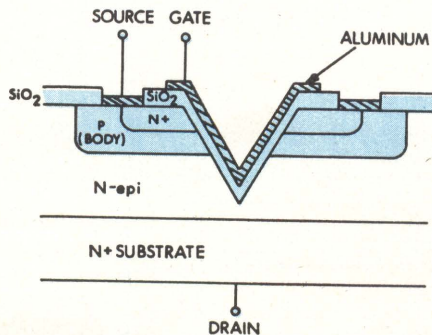
Since it is an insulated gate process, the only currents present at the input are leakages through the gate oxide and across the protection zener. This accounts for the low input current requirement. Because the devices use majority carrier technology, they are free of minority carrier storage time and base transit time. This allows switching speeds of 4 ns to be achieved, as opposed to the 0.5 to 2 μ s experienced with bipolar technologies.

Another attribute is that the transistors decrease their drain current as the junction temperature increases. This negative temperature coefficient allows devices to be paralleled without ballasting resistors and increases their reliability, eliminating the dangers of current hogging and thermal runaway associated with bipolar transistors. There is no need to derate current as operating voltage increases, because devices are not subject to secondary breakdown.

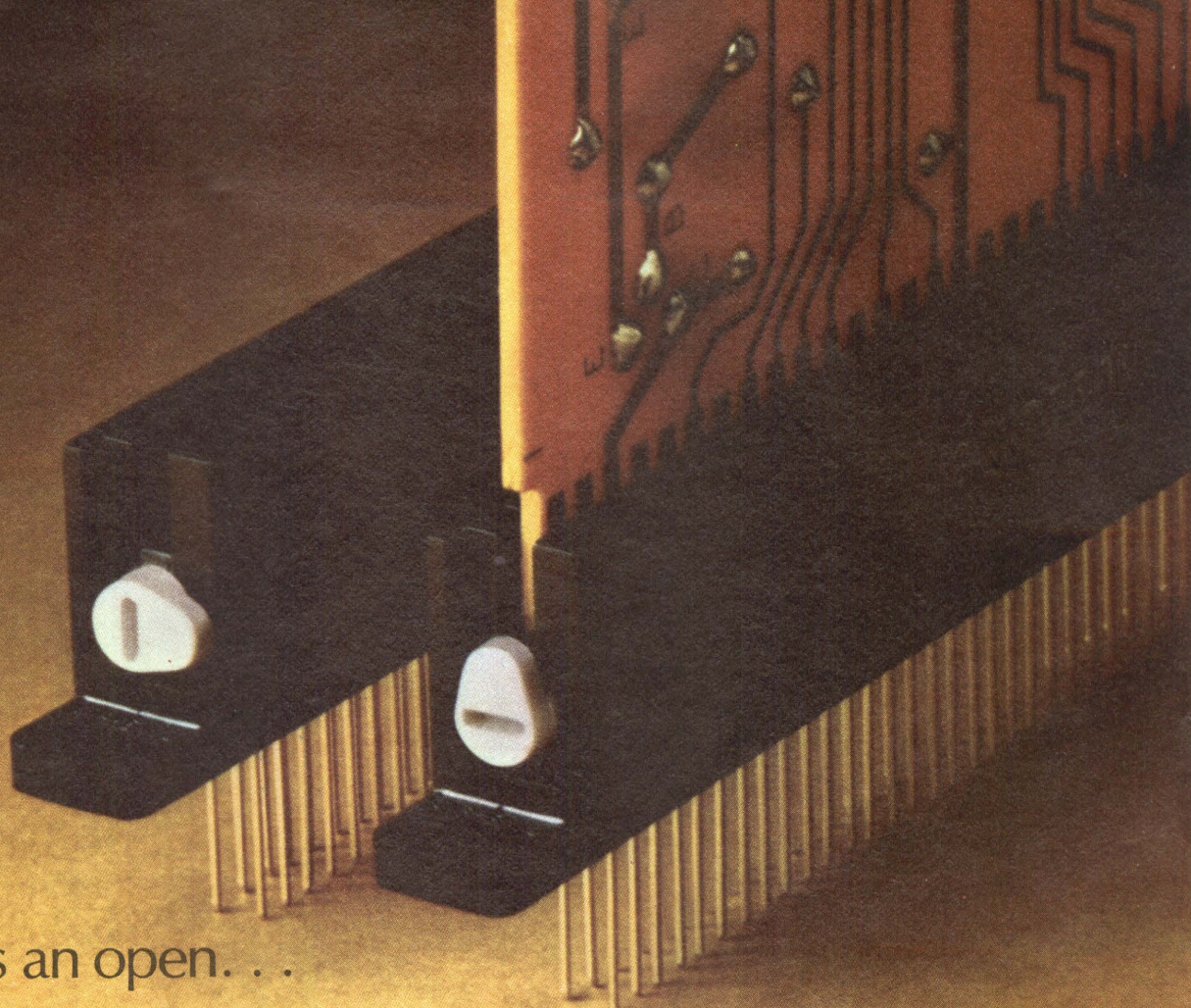
Other assets are ability to switch 1 A in less than 4 ns—an order of



Waveform observed on CMOS gate input and output drain connection of Siliconix' VN66AF Power FET shows switching times achieved using single NAND gate to drive 1-A switch. Rise time delays result from single gate's difficulty in pulling down device's approximately 40-pF input capacitance



Vertical MOS technology produces vertical current flow and provides greater current densities than planar MOS technologies. MOS gate is fabricated in V-groove etched through transistor body resulting in very short channel lengths



It's an open. . .

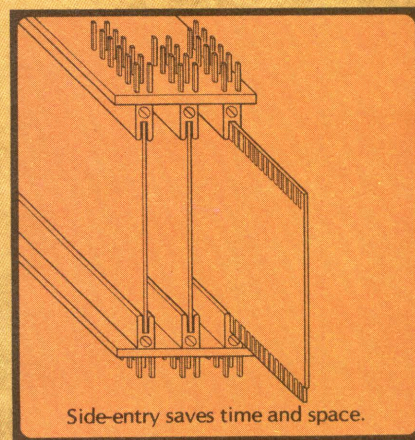
and shut case for

Amphenol ZIF connectors.

Easy does it with ZIF (Zero Insertion Force). Amphenol 244 Series connectors eliminate wear and tear on sensitive PC boards. Just a quarter-turn of the activating rod opens twin rows of cantilevered contacts. Insert the board, turn the rod back, and the contacts close—without damage to the board. Connection is secure, with 50 grams of force per contact.

Side-entry for high-density packaging. Two Amphenol ZIF connectors mounted perpendicular to a third can connect a board with readouts on three edges. Terminate as many as 228 circuits in the time and space it usually takes for 76 circuits.

Open up the possibilities. Get all the facts. Amphenol 244 Series ZIF connectors have 38 contact positions (76 independent opposing circuits) with solderless wire-wrapping terminations. For data, call Bob Casiello, (312) 986-3729. Or write: Amphenol North America Division, Bunker Ramo Corporation, Dept. L-107, 900 Commerce Drive, Oak Brook, Illinois 60521.



Side-entry saves time and space.

The right idea
at the
right time.



AMPHENOL®

CIRCLE 30 ON INQUIRY CARD

Motorola's introducing microcomputer system

1977 MPU family introductions

<input checked="" type="checkbox"/> MC3870P One-Chip Microcomputer	<input checked="" type="checkbox"/> MC68A21P Peripheral Interface Adapter	<input checked="" type="checkbox"/> MC68A50L Asynch. Comm. Interface Adapter	<input type="checkbox"/> MC68A488L General-Purpose Interface Adapter
<input checked="" type="checkbox"/> MC3870CP One-Chip Microcomputer	<input checked="" type="checkbox"/> MC68A21L Peripheral Interface Adapter	<input checked="" type="checkbox"/> MC68B50P Asynch. Comm. Interface Adapter	<input type="checkbox"/> MC68B488P General-Purpose Interface Adapter
<input checked="" type="checkbox"/> MC3870L One-Chip Microcomputer	<input checked="" type="checkbox"/> MC68B21P Peripheral Interface Adapter	<input checked="" type="checkbox"/> MC68B50L Asynch. Comm. Interface Adapter	<input type="checkbox"/> MC68B488L General-Purpose Interface Adapter
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<input checked="" type="checkbox"/> MC6800P Microprocessor	<input type="checkbox"/> MC6821MTL Peripheral Interface Adapter	<input type="checkbox"/> MC6850ML Asynch. Comm. Interface Adapter	<input checked="" type="checkbox"/> MC6830P 1K ROM
<input type="checkbox"/> MC6800CP Microprocessor	<input type="checkbox"/> MC6821ML Peripheral Interface Adapter	<input checked="" type="checkbox"/> MC6852P Synchronous Serial Data Adapter	<input type="checkbox"/> MCM6830CL 1K ROM
<input type="checkbox"/> MC6800MTL Microprocessor	<input checked="" type="checkbox"/> MC6840P Programmable Timer	<input type="checkbox"/> MC6852CP Synchronous Serial Data Adapter	<input type="checkbox"/> MCM68A30P 1K ROM
<input type="checkbox"/> MC6800ML Microprocessor	<input type="checkbox"/> MC6840CP Programmable Timer	<input type="checkbox"/> MC68A52P Synchronous Serial Data Adapter	<input type="checkbox"/> MCM68A30L 1K ROM
<input checked="" type="checkbox"/> MC68A00P Microprocessor	<input checked="" type="checkbox"/> MC6840L Programmable Timer	<input type="checkbox"/> MC68A52L Synchronous Serial Data Adapter	<input type="checkbox"/> MCM68B30P 1K ROM
<input checked="" type="checkbox"/> MC68B00P Microprocessor	<input type="checkbox"/> MC6840CL Programmable Timer	<input type="checkbox"/> MC6852MTL Synchronous Serial Data Adapter	<input type="checkbox"/> MCM68B30L 1K ROM
<input checked="" type="checkbox"/> MC68A00L Microprocessor	<input type="checkbox"/> MC68A40P Programmable Timer	<input checked="" type="checkbox"/> MC6854P Advanced Data Link Controller	<input checked="" type="checkbox"/> MCM68308P 8K ROM
<input checked="" type="checkbox"/> MC68B00L Microprocessor	<input type="checkbox"/> MC68A40L Programmable Timer	<input type="checkbox"/> MC6854CP Advanced Data Link Controller	<input checked="" type="checkbox"/> MCM68308L 8K ROM
<input checked="" type="checkbox"/> MC6802P Microprocessor + RAM & Clock	<input type="checkbox"/> MC68B40P Programmable Timer	<input checked="" type="checkbox"/> MC6854L Advanced Data Link Controller	<input type="checkbox"/> MCM68308CL 8K ROM
<input type="checkbox"/> MC6802CP Microprocessor + RAM & Clock	<input type="checkbox"/> MC68B40L Programmable Timer	<input type="checkbox"/> MC6854CL Advanced Data Link Controller	<input type="checkbox"/> MCM68A308P 8K ROM
<input checked="" type="checkbox"/> MC6802L Microprocessor + RAM & Clock	<input type="checkbox"/> MC6840MTL Programmable Timer	<input type="checkbox"/> MC68A54P Advanced Data Link Controller	<input type="checkbox"/> MCM68A308L 8K ROM
<input type="checkbox"/> MC6802CL Microprocessor + RAM & Clock	<input type="checkbox"/> MC6843P Floppy Disk Controller	<input type="checkbox"/> MC68A54L Advanced Data Link Controller	<input type="checkbox"/> MCM68316AP 16K ROM
<input checked="" type="checkbox"/> MCM6810P Byte-Organized RAM	<input type="checkbox"/> MC6843L Floppy Disk Controller	<input type="checkbox"/> MC68B54P Advanced Data Link Controller	<input type="checkbox"/> MCM68316AL 16K ROM
<input type="checkbox"/> MCM6810CP Byte-Organized RAM	<input type="checkbox"/> MC6844P DMA Controller (1.0 MHz)	<input type="checkbox"/> MC68B54L Advanced Data Link Controller	<input checked="" type="checkbox"/> MCM68316EP 16K ROM
<input checked="" type="checkbox"/> MCM68A10P Byte-Organized RAM	<input type="checkbox"/> MC6844L DMA Controller	<input type="checkbox"/> MC6854MTL Advanced Data Link Controller	<input checked="" type="checkbox"/> MCM68316EL 16K ROM
<input checked="" type="checkbox"/> MCM68A10L Byte-Organized RAM	<input type="checkbox"/> MC6845P CRT Controller	<input checked="" type="checkbox"/> MC6860P 0-600 bps Modem	<input type="checkbox"/> MCM68A316EL 16K ROM
<input checked="" type="checkbox"/> MCM68B10P Byte-Organized RAM	<input type="checkbox"/> MC6845L CRT Controller	<input checked="" type="checkbox"/> MC6862P 2400 bps Modulator	<input checked="" type="checkbox"/> MCM68708L 8K EPROM
<input checked="" type="checkbox"/> MCM68B10L Byte-Organized RAM	<input type="checkbox"/> MC6846P MC6802 Combo	<input type="checkbox"/> MC6875P Clock Oscillator/Driver—	<input checked="" type="checkbox"/> MCM68A708L 8K EPROM
<input type="checkbox"/> MCM6810MTL Byte-Organized RAM	<input type="checkbox"/> MC6846CP MC6802 Combo	<input type="checkbox"/> MC6875L Clock Oscillator/Driver—	
<input type="checkbox"/> MCM6810ML Byte-Organized RAM	<input type="checkbox"/> MC6846L MC6802 Combo	<input type="checkbox"/> MC68488P General-Purpose Interface Adapter	
<input checked="" type="checkbox"/> MC6821P Peripheral Interface Adapter	<input type="checkbox"/> MC6846CL MC6802 Combo	<input type="checkbox"/> MC68488CP General-Purpose Interface Adapter	
<input type="checkbox"/> MC6821CP Peripheral Interface Adapter	<input checked="" type="checkbox"/> MC6850P Asynch. Comm. Interface Adapter	<input type="checkbox"/> MC68488L General-Purpose Interface Adapter	
<input checked="" type="checkbox"/> MC6821L Peripheral Interface Adapter	<input type="checkbox"/> MC6850CP Asynch. Comm. Interface Adapter	<input type="checkbox"/> MC68488CL General-Purpose Interface Adapter	
<input type="checkbox"/> MC6821CL Peripheral Interface Adapter	<input checked="" type="checkbox"/> MC68A50P Asynch. Comm. Interface Adapter	<input type="checkbox"/> MC68A488P General-Purpose Interface Adapter	

☒ Introduced
☐ Introducing Now
☐ To Be Introduced

Frequency Range
 MC68XX = 1.0 MHz
 MC68AXX = 1.5 MHz
 MC68BXX = 2.0 MHz

Temperature
 MC68XX = 0° C to +70° C
 MC68XXC = -40° C to +85° C
 MC68XXMT = -55° C to +125° C
 MC68XXM = MIL-883

Package
 MC68XXP = Plastic
 MC68XXL = Ceramic
Pin-Out Variations
 Suffix A, Suffix E

2nd Quarter, 1978

☐ MC6801
Microprocessor

3rd Quarter, 1978

☐ MC6809
Microprocessor

over 100 compatible components this year.

Here's #41: MC6854 - the full capability Advanced Data Link Controller (ADLC)

Our newest addition to the M6800 Family, the ADLC provides the key interface and control between an 8-bit parallel data bus and a serial synchronous data communications line of either NRZ or zero complementary NRZI operation. The MC6854 makes this complex job easy for both primary and secondary stations, in point-to-point or loop configurations.



The MC6854 ADLC is **compatible with all bit-oriented protocols**

such as Advanced Data Communication Control Procedure (ADCCP), High-Level Data Link Control (HDLC) and Synchronous Data Link Control (SDLC). It receives and transmits data frames in half and full duplex, and provides a variety of automatic features including flag generation and detection, CRC generation and verification, and zero-bit insertion and deletion. Loop mode gives the ADLC extra capability in gaining and relinquishing loop control.

A data frame is composed of the opening flag, address field, control field, information field, frame check sequencer field and closing flag. It automatically initiates with open flag and closes with FCF and close flag.

Of course the MC6854 is M6800-compatible, with 8-bit bi-directional data bus, chip select lines, register select lines, interrupt request, read/write line, an enable line and a reset line. It has four bytes of buffering on both

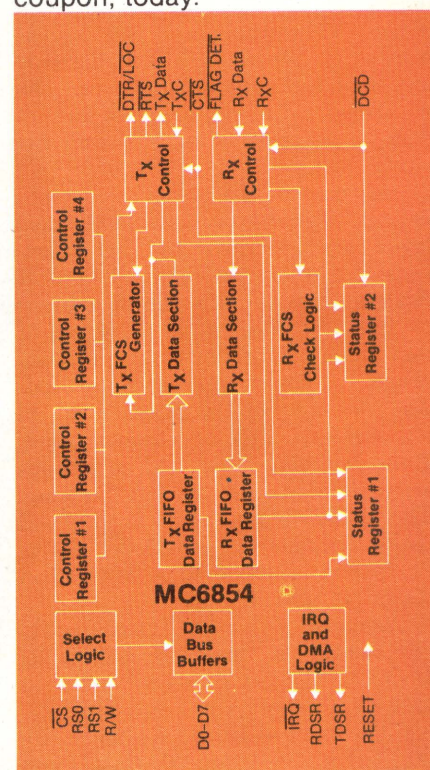
transmit and receive. It has DMA request lines, modem control lines and loop control lines. The data rate is up to one megabit. Information field data can be anywhere from five to eight bits per byte, and the device features automatic extension mode for each address, link control and logical control field. Both plastic and ceramic versions of the MC6854 are engineered into a space-saving 28-pin package for lowest cost and maximum space efficiency. It's a super ADLC.

Our massive MPU commitment is paying off.

More than 100 new parts in one year. New families like the 1.5 MHz and 2.0 MHz '68A00 and '68B00. An improved series of peripheral interface adapters. A two-chip system like the MC6802-MC6846. A programmable timer. And now the ADLC, plus many outstanding developments yet to come by December, '77, and on into '78 as well. All hardware, software and bus-compatible. With an MOS center of excellence in Austin, Texas, and manufacturing and

second-sourcing on three continents.

Let us demonstrate how Motorola's global commitment to the MPU market can serve your microcomputer needs. Send in the coupon, today.



To: MOTOROLA SEMICONDUCTOR PRODUCTS, INC.

DIRECT ACTION

Motorola Microproducts, 3501 Ed Bluestein Blvd., Austin, Texas 78721

I have an immediate requirement. Please call me. Phone _____

My application is: _____

NAME _____ TITLE _____

FIRM _____ DEPT. _____

ADDRESS _____

CITY/STATE/ZIP _____



MOTOROLA Semiconductors
The mind to imagine... the skill to do.

magnitude faster than a bipolar with similar current capabilities; low input resistance at radio frequencies, which opens up broadband opportunities; and low radio frequency noise figures, which make it competitive with any transistor for small signal receivers or high power transmitter applications.

A normally-off device when input is at ground and a fully-on device which draws no input current when input is high, the VN66AF shows no offset voltage under low load conditions. When used to replace Darlington bipolar devices, the device achieves significant parts savings. In one example, 24 vmos devices replaced 72 resistors and 48 bipolar transistors. Where high load currents are required, the devices can be paralleled with no need to insure even distribution of load current between devices.

Also constructed using vmos technology, 2N6657 and 2N6660 have lower input current and lower on-resistance than the VMP 1 and 2 devices they replace. Input current of 100 nA results in less loading of the driver; 2.5-Ω max on-resistance results in lower power dissipation. The devices handle currents up to 3 A and have 60-V breakdown rating, 10-ns switching times, and no secondary breakdown or current hogging. The 2N6657, packaged in a TO-3 pack, is capable of 25-W power dissipation; 2N6660 in a TO-39 can dissipates 6.25 W.

Packaged in plastic TO-202 package which is machine insertable, VNXXAF devices save on initial cost and on assembly costs. Specified according to breakdown voltages—40, 60, and 80 V—VN46AF, 66AF, and 88AF are all rated at 12.5-W dissipation and are guaranteed over the —55 to 150°C temperature range.

Circle 143 on Inquiry Card

Tape Recorder Uses 70 Tracks/in Head To Record 240M Bits/s

A 240M-bit/s tape recorder, representing a dramatic advance in high rate digital recording, uses a high performance, 70-track/in magnetic head and provides area packing density on tape of more than 1.5M bits/in/ (0.2M bits/cm²). Demonstrated by RCA Government Recording Systems, Camden, NJ 08102, the high

density multitrack recording (HDMR) recorder will enable real-time, direct digital recording of wideband sensors.

Developed with support from NASA's Office of Applications, HDMR is claimed to provide a 3-fold data rate advantage over currently available high speed digital recorders. Previously, rates greater than 100M bits/s could be handled only by using several synchronized transports. The single transport recorder allows system designers to consider completely digital wideband systems. Near term applications exist in the space shuttle, and for recording data from satellite-borne earth sensing equipment.

Next step is refinement of the laboratory tape transport and further development of higher density recording heads. These efforts will be aimed at achieving single-transport tape systems capable of handling data at serial transfer rates in excess of 1G bits/s.

Circle 144 on Inquiry Card

Products Expand Distributed Data Processing Capabilities

Six products intended to expand the capability of Series 21 systems in distributed processing include a compatible channel for interfacing to larger systems, three printers covering the 90- to 600-line/min range, and two magnetic tape drives for converting diskette media. Mohawk Data Sciences Corp, 1599 Littleton Rd, Parsippany, NJ 07054 designed the compatible channel to provide systems users with all elements necessary for a distributed processing network.

The channel (Feature 180) allows Series 21 systems to interface directly with larger MDS 1200, 2300, and 2400 systems. For example, connected to an RJE terminal, such as the System 2300 HASP interleaving workstation, via the channel, a system serves to replace the keypunch units usually surrounding an RJE terminal. Through the interface, Series 21 computers can take advantage of System 2400 data communication capabilities, which include 11 industry-compatible communications emulators.

Offering users the ability to generate reports faster and more economically, the 2142-1 printer operates

at from 90 to 240 lines/min, the 2142-2 from 230 to 340 lines/min. In both units, print speed is dependent on the number of characters actually printed rather than the number of print positions. For a maximum of 132 printed characters/line, the units have speeds of 90 and 240 lines/min, respectively; with typical 75-character lines, they produce 150 and 340 lines/min, respectively.

Users gain a convenient method of converting diskette records to computer-compatible media by attaching a magnetic tape drive to the system. Model 2481 is a 9-track, 800-bit/in unit, while the 2482 is a 9-track, 1600 bits/in drive.

Circle 145 on Inquiry Card

English-Like Commands Simplify Operation of Graphics System

Tell-a-Graf produces publication quality, highly flexible graphics without requiring a computer expert. Based on the Disspla computer graphics system, also developed by Integrated Software Systems Corp, 4186 Sorrento Valley Blvd, Suite G, San Diego, CA 92121, the product minimizes communications problems by giving control of the end result to clerk, technician, or manager. The combination of a highly sophisticated language processor, interpreting "natural language" English-like commands, with the computer graphics system makes available the benefits of visual media—clarity, impact, and legibility—with substantially less effort.

To use the system, a user need only input brief commands, such as

Generate a bar chart with a monthly X axis. Label the Y axis "Dollars," the X axis "Year of 1970," and write the title "Acme Manufacturing" "Cost Evolution" in italic lettering. Frame the picture, and comment it "Source: Branch Office Reports."

Then he simply provides the input data to achieve the plot described. A legend is automatically generated, axes are scaled to fit, and headings and axes labels are positioned automatically. By simplifying the commands while allowing modifications and tailoring to fit special needs, the system reduces the procedure to a matter of furnishing data.

The system is currently offered for IBM virtual storage systems. It is also available on the NCSS national service bureau.

Circle 146 on Inquiry Card

Honeywell's Level 6.

The mini that lets you design aggressively for the future.

Honeywell's Level 6 minicomputer brings new design freedom to the OEM and systems builder.

With its fully open-ended, modular architecture and unique Megabus that lets you mix processors, memories, communications and peripherals to meet just about any system requirements.

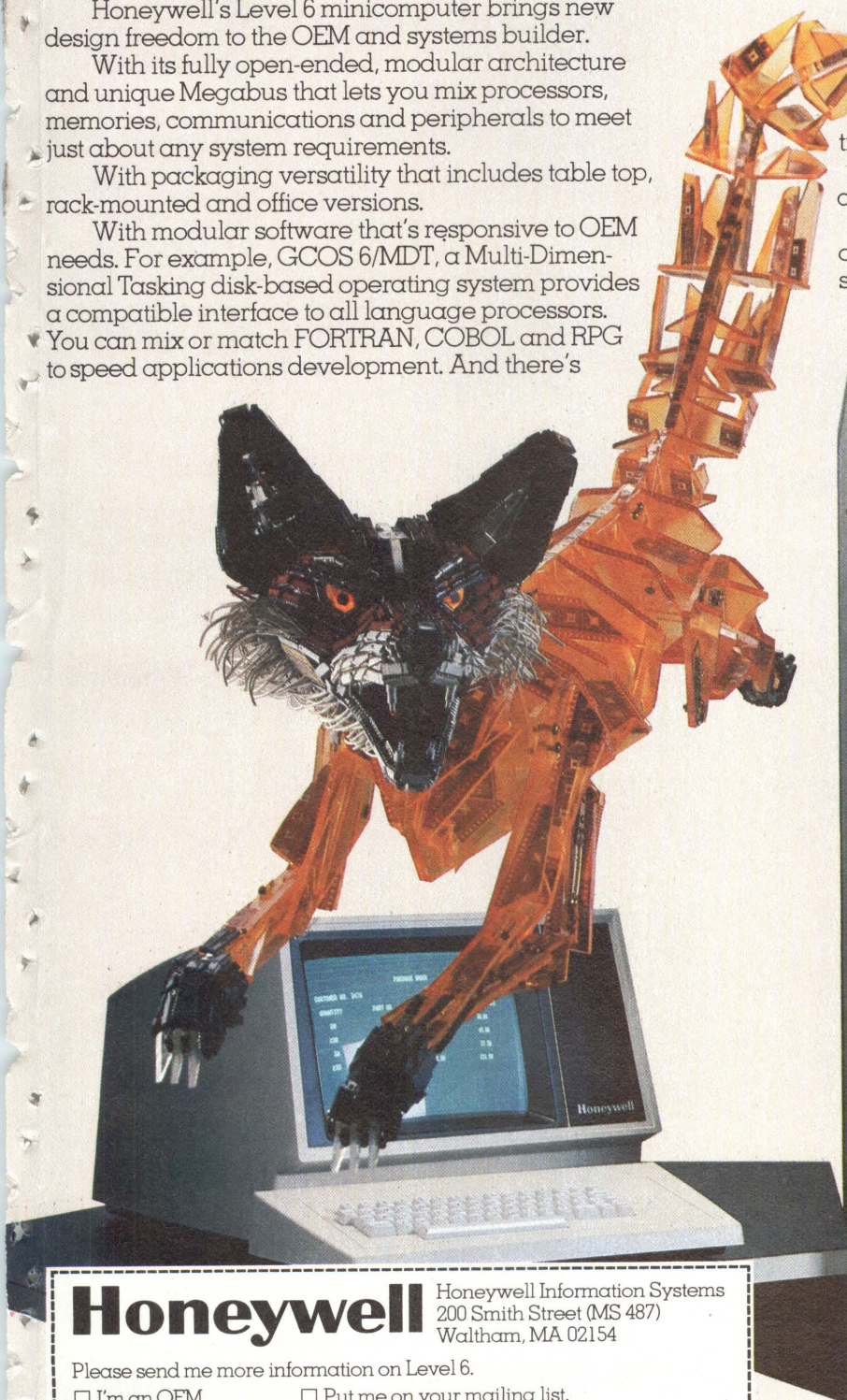
With packaging versatility that includes table top, rack-mounted and office versions.

With modular software that's responsive to OEM needs. For example, GCOS 6/MDT, a Multi-Dimensional Tasking disk-based operating system provides a compatible interface to all language processors. You can mix or match FORTRAN, COBOL and RPG to speed applications development. And there's

full compatibility between the ISAM file system and the language processors as well. Furthermore, GCOS 6/MDT takes full advantage of Level 6 hardware features such as automatic context save and restore, independent traps and dynamically assignable priority levels.

With our attractive OEM pricing, contracts, and policies.

And with a worldwide mainframe supplier on your team, when you need maintenance or support, you don't have to hunt for it.



Honeywell

Honeywell Information Systems
200 Smith Street (MS 487)
Waltham, MA 02154

Please send me more information on Level 6.

- | | |
|---|--|
| <input type="checkbox"/> I'm an OEM. | <input type="checkbox"/> Put me on your mailing list. |
| <input type="checkbox"/> I'm an end-user. | <input type="checkbox"/> I've read enough, let's talk. |

NAME _____

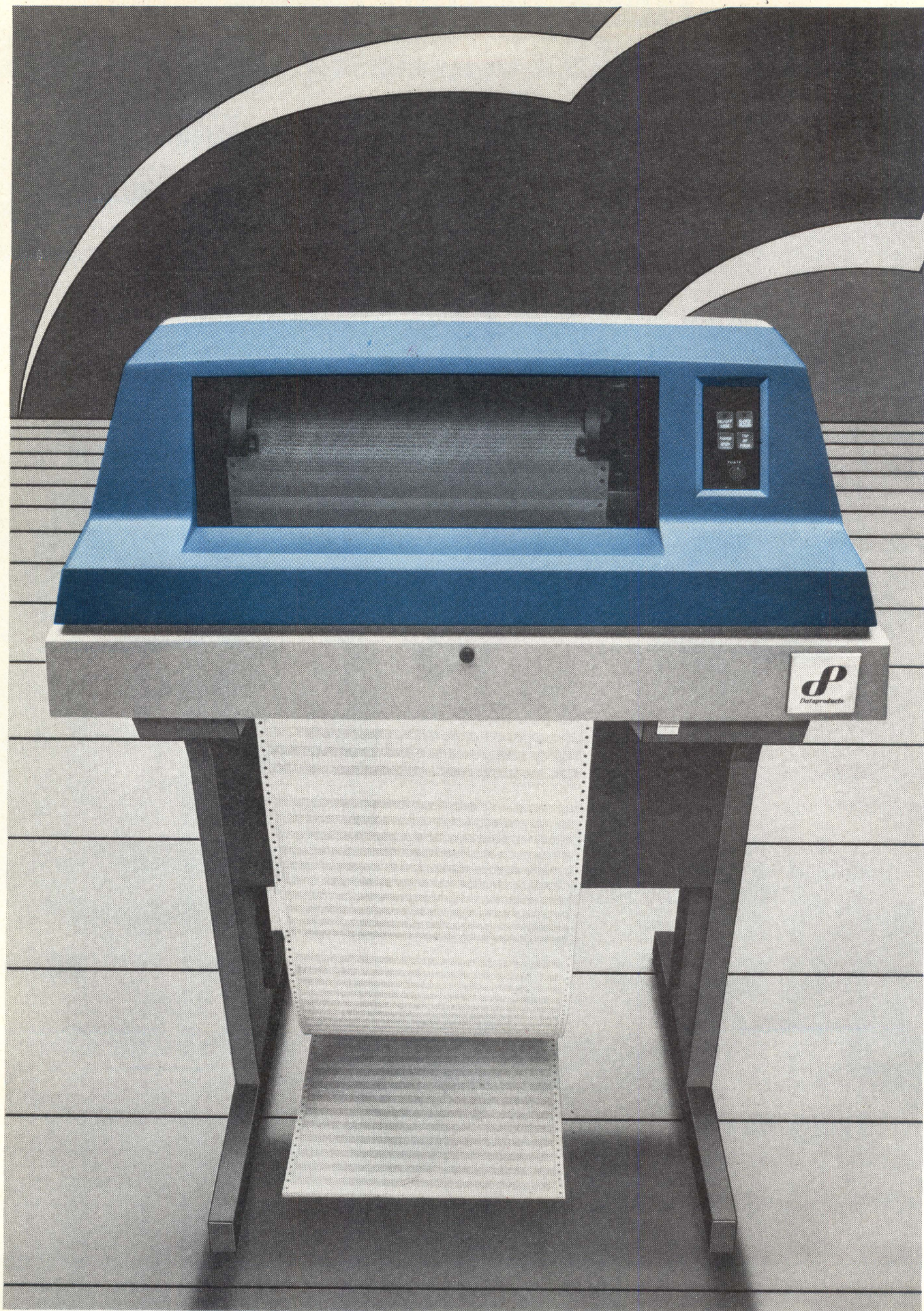
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COMPANY _____

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CITY _____ STATE _____ ZIP _____

We want you to have all the facts on Level 6.



DATAPRODUCTS' NEW ERA BAND PRINTERS: DEPENDABILITY AND ECONOMY.

Our B-Series band printers are the first in the industry with built-in Dataproducts dependability.

And versatility.

We built in a lightweight, operator-replaceable band so the end-user can print at either 10 or 15 character/inch spacing, with a variety of font styles.

We built in our patented, field-proven Mark V hammer system.

We built in ruggedness and low power consumption so our B-Series machines can perform to our high, self-imposed standards.

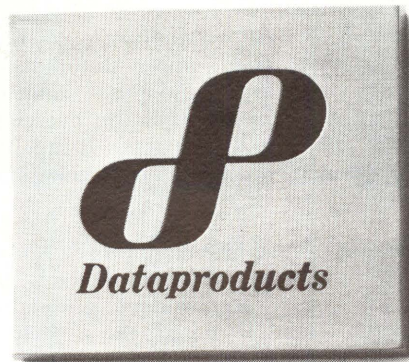
And we built in an exclusive diagnostic display to maximize uptime and minimize unnecessary service calls.

Finally, we built both the B-300 model (at 300 LPM) and the B-180 model (at 180 LPM) so compact that they can be used on a table top or on a pedestal.

But most important to OEMs and end-users, we built in economy.

Ask for more information and you'll be convinced a New Era in band printing is here.

Then join the Dataproducts bandwagon.



THE PRINTER COMPANY

NORTH AMERICAN SALES HQ: 6219 De Soto Avenue, Woodland Hills, CA 91365, (213)887-8451; Telex 69-8492.
EUROPEAN SALES HQ: Darmstaedter Landstrasse 199, Frankfurt, W. Germany, Phone 681034; Telex 841-416344.

CIRCLE 33 ON INQUIRY CARD

Plasma Display Terminals Provide Competition For Full Performance CRTs

PD series plasma display terminals incorporate advances in mechanism and electronics, at less cost. Through use of extensively redesigned circuits implemented with ICs, unit weight of the terminal is kept under 40 lb (18 kg) and the 24" (61 cm) depth has been reduced to 12" (30 cm).

Introduced by Interstate Electronics Corp, 707 E Vermont Ave, PO Box 3117, Anaheim, CA 92803, models PD 1000 and 2000 use a single sustaining waveform voltage, rather than the dual voltage of previous models, eliminating synchronization problems. Matrix points are driven by special ICs, and a 12-chip microprocessor simplifies the communication link to the computer and increases the data transfer rate to 10,200 baud.

Standard features include dual font upper and lower case alphamerics, full graphics capability, interactive keyboard, and extensive control command functions. A standard RS-232-C I/O port allows serial data rates from 150 to 19,200 baud. Maximum writing rate for 5 x 7 characters is 8333 char/s. Optional are a second serial port and a 16-bit parallel I/O port, which allows data transfer at a minimum of 167,000 words/s.

The memory-display array in a plasma panel consists of two sets of parallel conductor lines, each printed on a sheet of glass and positioned at right angles to each other. A panel with 512 horizontal and 512 parallel lines has 262,144 intersection points, each defined by a particular combination of two conductor lines.

The two glass plates are positioned a precise distance from each other and the space is filled with neon gas. An oscillating voltage, below the threshold needed to ionize the gas, is applied across the gap. When an extra voltage is applied across two intersecting lines, a glowing plasma path is established and is sustained by the lower level voltage. This dot can be extinguished by dropping the voltage across the intersecting lines below the sustaining level.

With a typical pattern of 60 lines/in (24/cm) on both horizontal and vertical plates, plasma dots have a diameter of approximately 10 mils. Resolution is sufficient for alphanu-

meric and graphic display applications. Bright neon orange color provides a 20:1 contrast ratio, while the flat display plate eliminates distortions and provides a wide viewing angle. Dots can be added and subtracted at a rate of 50k/s. The sustaining voltage oscillates at the same rate, producing a flicker-free image.

PD 2000 is offered with a military quality package and uses ceramic ICs to meet industrial and sheltered military requirements. PD 1000 has computer-grade components. Both terminals can be equipped with a microfiche projector controllable from the computer or the terminal keyboard. Price of the 1000 ranges from \$8900; the 2000 from \$10,000.

Circle 147 on Inquiry Card

Noninterruptive System Provides Constant Power Mechanically

Noninterruptive power system (UPS) modules totally isolate computer systems from the power line, absorbing power disturbances to provide protection from blackouts and brownouts. Development of a variable-speed precise frequency generator by Precise Power Corp, PO Box 1905, Bradenton, FL 33506 has provided the technology necessary. The rotary UPS provides long operating life, minimal maintenance, crystal-controlled frequency, and is not rate limited. No batteries are used, eliminating the need for special venting systems and floor space requirements.

In normal operation, utility/power lines provide power to an electric motor which is coupled to a variable speed/precise frequency generator. The generator provides all power to the computer installation, absorbing any high speed power disturbance, such as severe lightning induced transients, dips, surges, or overvoltages. Because the generator is capable of producing constant frequency and voltage as it slows down, the unit offers 10 to 30 s of power-out ride-through capability at full load. Longer protection can be attained by switching to a gas-driven generator.

The unit is based on a simple induction motor which is mechanically shafted to the frequency generator. This generator has a continuous layer of magnetizable material lined around the rotor periphery. As the

rotor turns at a nominal operating speed, an exciter head mounted on the stator continuously writes the poles on the magnetic material. Excitation for the writing head is provided by a precision oscillator and amplifier. If machine speed varies, the writing head varies the spacing of the poles so that the stator coils see the same number of poles per second in spite of the speed variation.

Modular construction allows users to choose how much conditioning they need and to add capability as required. Working units are supplied ready to run; several modules run in parallel will accommodate large systems.

Circle 148 on Inquiry Card

Software System for Data Protection Through Encryption

An advanced software system that provides data protection through encryption has been released for use on IBM Systems 360/370. Developed by Hansco Data Processing, PO Box 236, Wilbraham, MA 01095, the package is available in two versions: Civilian/007 and Federal/007. Both are based on complicated mathematical manipulations and employ a user-supplied 8-byte activating key, allowing up to 1.7×10^{18} possible ciphers.

Civilian/007 protects data through a 2-state algorithm. It is so sensitive that minute variations in key composition or record content cause vast differences in encrypted output. As such, the package acts as a convenient deterrent to curious programmers, operators, systems programmers, and industrial spies.

Federal/007 is a software implementation of the Federal Data Encryption Standard (DES) now required by the federal government for sensitive and valuable data. According to the U.S. Bureau of Standards, the DES algorithm so confounds the original data that "no other technique other than trying all possible keys using known input and output for the DES will guarantee finding the chosen key" (FIPS publication 46, Jan 15, 1977).

Both versions are implemented in user programs via standard subroutine calls and are self-relocating and re-entrant, providing language and operating system independence as well as maximum flexibility. Packages are priced at \$495 each, and come with complete documentation and maintenance. □

Circle 149 on Inquiry Card



How to turn a computer into a disk jockey. The μ PD372 Floppy Disk Controller.

Now you can turn almost any micro or minicomputer into a genuine floppy disk jockey with the help of just one small chip.

Our μ PD372 Floppy Disk Controller. Or if your computer prefers playing tapes, we also have the μ PD371 Tape Cassette Controller.

Either one can take the place of from 50 to 60 TTL packages to save you space as well as money. The 372 is

completely compatible with IBM, Minifloppy,TM* and other formats and controls up to 4 floppy disk drives. The 371 controls up to 2 tape cassette drives. They come with complete documentation and—best of all—they're available now.

The μ PD372 and 371 are just part of our complete family of micro-processor products including 8080As, dynamic and static RAMs, ROMs,

Electrically Erasable PROMs, and 8212, 8214, 8216, 8224, 8228/38, 8251, 8255 and other support chips. All backed by full documentation, applications support, and software.

The μ PD372. The μ PD371. And the hits just keep on comin'.

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It's easy to inspect, test and repair
AMP Latch multi-conductor
connectors.

Even after they're in use.





We designed them that way. Because a mass termination connector should help you save time and effort before, during and after assembly.

Their unique folded contact design, with dual camming and latching ears, assures you of four-point electrical contact and mechanical grip for each conductor. And that means superior overall reliability and protection. In addition, these fork-type contacts make it especially easy to visually inspect each termination before the cover is applied.

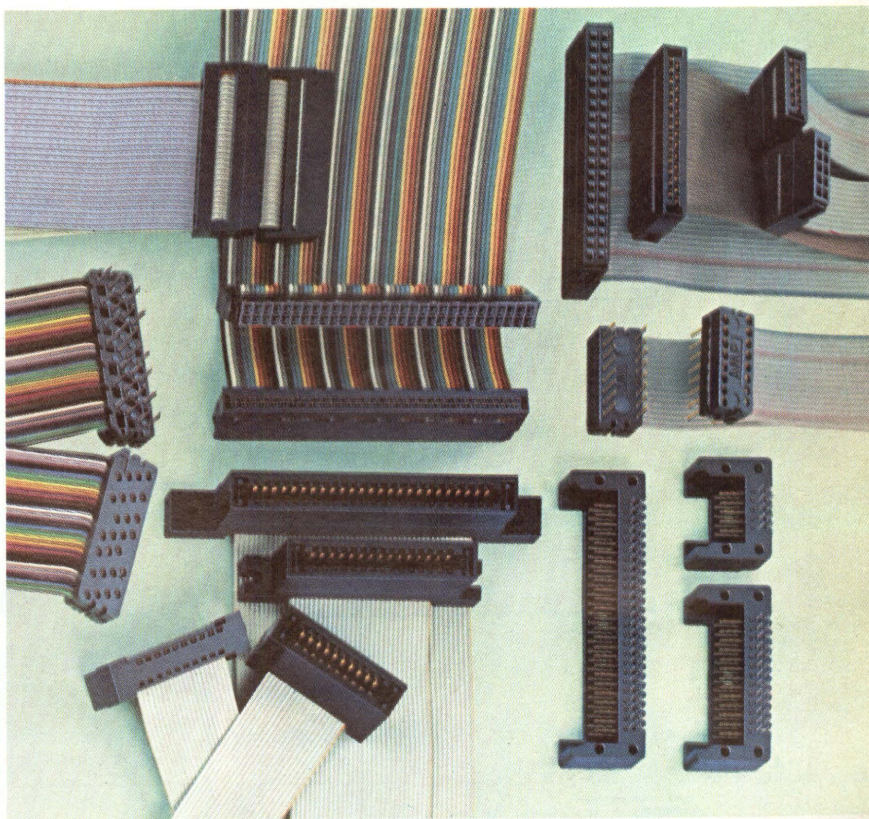
And even after the cover is on, each contact can still be visually checked for proper locking and latching. Because every AMP Latch cover has a built-in inspection port over each termination. This also permits electrical testing without cover removal, saving additional production time. And if repair ever is necessary, we've made that easier, too, by designing special hand and pen tools.

There are more reasons why you should choose AMP Latch connectors such as quick, easy terminating with the AMP shuttle tool, and the broad variety of pin headers and connectors. You also get AMP backup . . . expert design and production help that's yours for the asking from AMP connector engineers.

Why not contact Customer Service, at (717) 564-0100 for complete details on the AMP Latch connector line? Or write us direct. AMP Incorporated, Harrisburg, PA 17105.

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CIRCLE 34 ON INQUIRY CARD

Computer-Directed Warehouse System Relieves Personnel by Locating Parts and Maintaining Paperwork

As the number of available models for any product line increases, the replacement parts necessary to be warehoused multiply rapidly. More and more items to be stocked results in bigger and bigger warehouses—which in turn means that it becomes harder and harder to find and access those items quickly and efficiently. For example, Mercury Marine, an outboard motor supplier, must fill 500 orders a day, which amounts to locating and picking 4500 items from 25,000 stocked in its warehouse.

To enable rapid fulfillment of these functions, Mobility Systems, Inc of Greene, NY 13778 designed and installed an order picking system featuring a group of vehicles which roam the floors of the warehouse under the direction of a minicomputer. This computer routes traffic, selects the order of picking, determines size and order location of parts, updates inventory, redirects vehicles to other locations if one location is

out of parts, prints packing labels for filled orders, and back orders parts that are out of stock. A rider on each vehicle removes items from stock or adds them to inventory on instructions from the computer that are displayed on a CRT on the vehicle.

Functional Description

Mobility warehouse control systems are available in a variety of configurations to permit adaptation to specific requirements. However, the fundamental design goal is to relieve warehouse personnel from the dual burdens of locating items and of handling paperwork. Systems are used both to pick parts to fill orders and to restock the bins and racks.

A basic M/2000 system consists of material handling equipment (MHE)—vehicles which move from one storage location to another—and computer control devices. The specific Mercury Marine installation contains both

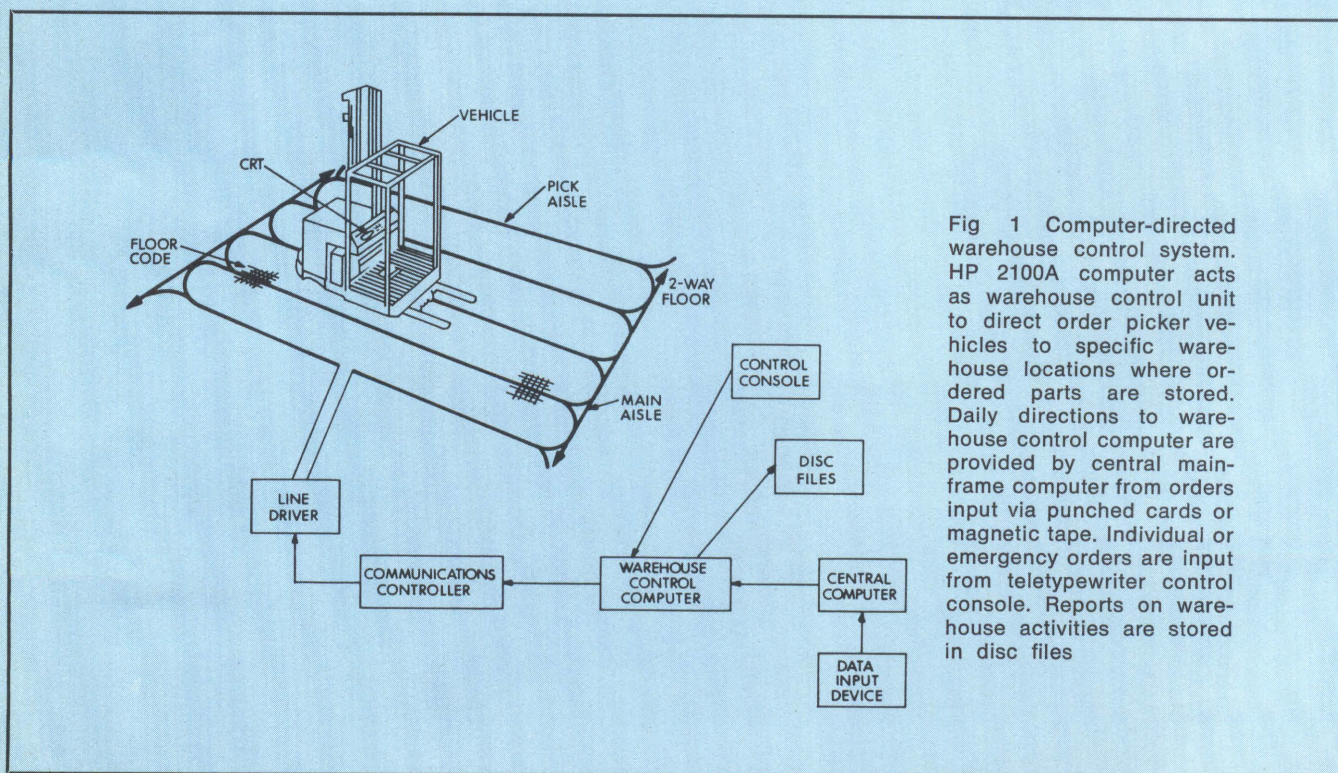


Fig 1 Computer-directed warehouse control system. HP 2100A computer acts as warehouse control unit to direct order picker vehicles to specific warehouse locations where ordered parts are stored. Daily directions to warehouse control computer are provided by central mainframe computer from orders input via punched cards or magnetic tape. Individual or emergency orders are input from teletypewriter control console. Reports on warehouse activities are stored in disc files

Pick a signal and any mini...Using RTP

Let's say you have some relay contacts to monitor, 115 VAC control signals to sense, 4 to 20 mA analog process signals to measure, and you need to provide relay output contact closures and 4 to 20 mA set-point signals.

This application can be handled by a few standard RTP analog and digital input/output cards, a Universal Controller, and an RTP Bus Converter.

First, you select the cards. Our family of process I/O interface cards provides the versatility to match almost all industrial sensors and actuators.

The Universal Controller provides the logic, power and space for up to 16 of these cards, in any combination.

The RTP Bus Converter interfaces the Universal Controller to your mini by con-

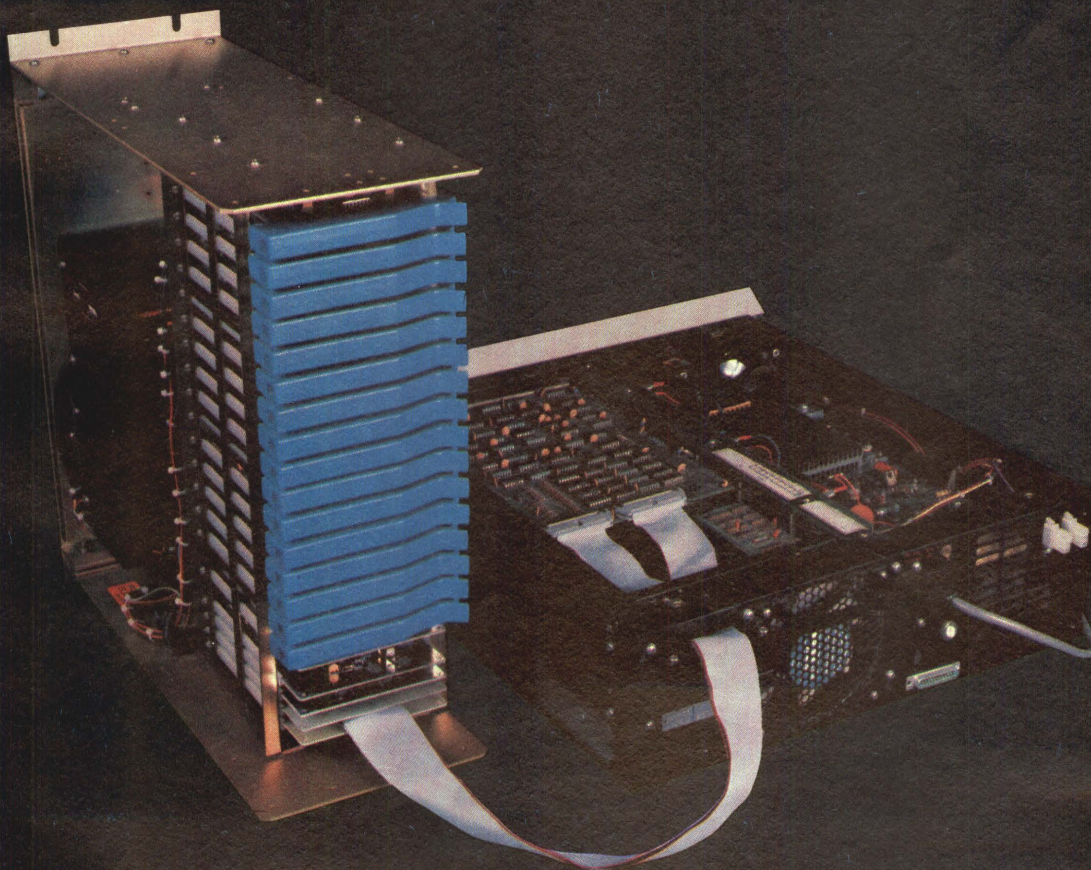
verting your mini's parallel I/O bus to the standard RTP parallel bus. Appearing transparent to your computer, it allows the Universal Controller to be directly programmed, as if it were one of the computer's peripherals. Best of all, RTP Bus Converters are available for all popular minicomputers.

Those are the essentials! But it's kind of tough to design a measurement and control system from an ad.

So, we'd like to send you "Using RTP." This booklet will provide you with a concise RTP subsystem design overview. Just circle our number on the Reader Service Card.



Computer Products, inc.

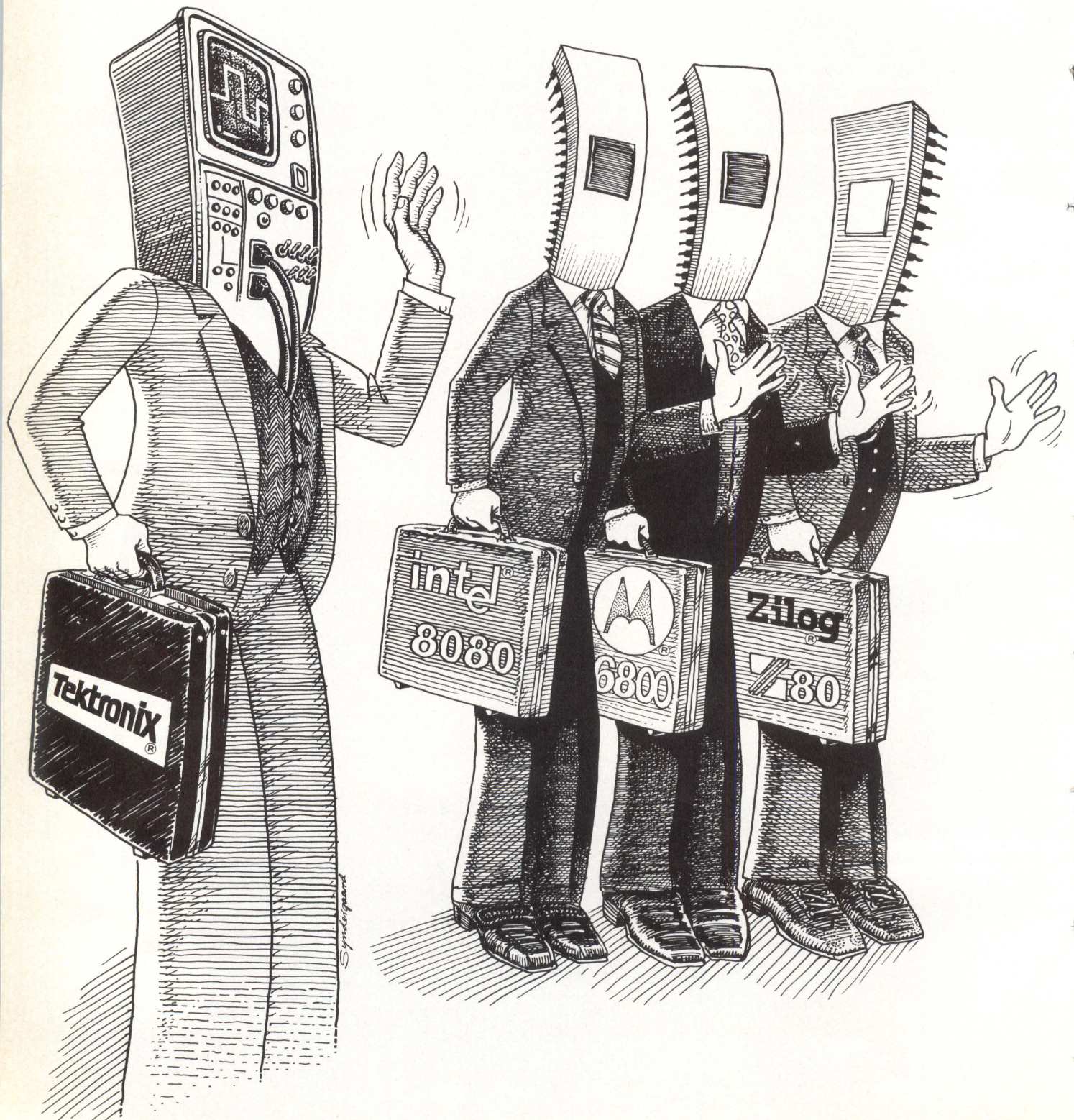


I/O Versatile

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CIRCLE 35 ON INQUIRY CARD

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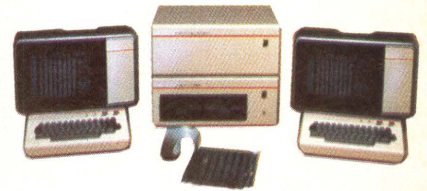
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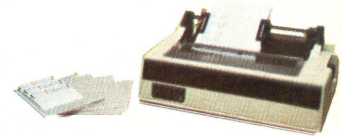
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CIRCLE 36 ON INQUIRY CARD

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computer-controlled order picker and stocker MHE vehicles which operate within a 130,000-ft² (12,000-m²) area, and noncomputer-controlled side-reach pallet handlers which move large parts or pallets within the remainder of the 216,000-ft² (20,000-m²) warehouse.

Warehouse control is maintained by a Hewlett-Packard 2100A computer with 24k words of memory, two 5M-byte HP 7900A magnetic disc storage systems, a 1600-bit/in (630-bit/cm) magnetic tape data input system, and a modified teletypewriter control console. A communications controller provides interface between computer and vehicles over an rf channel, and a 300-line/min printer prepares packing lists after ordered parts are ready for shipment.

When incoming orders are received, cards are punched and accumulated for two daily inputs to the company's central mainframe computer (Fig 1). As cards are processed on that computer, parts are allocated from stock on hand. Each day, distribution management determines the orders to be picked, first filling backorders and then new orders, and instructs the data processing department to arrange those orders into runs, in a procedure called "run and module makeup."

As part of the run and module makeup, the mainframe computer calculates the cube (the space to be occupied) of all orders and assigns each order to the first slot which it will fit in the stocking module carried on the MHE vehicle. This process continues, assigning the lowest priority orders to any remaining vacant slots, until the module is filled or all orders have been handled. Parts in each order assigned to the module are arranged by warehouse location sequence for shortest run time, and a picking run number is chosen. Any parts not in the computer-controlled area are entered on cards for manual picking from another part of the warehouse. The rest go onto magnetic tape and are loaded into the warehouse control computer for assignment to order picking vehicles.

Bins and racks in the computer-controlled portion of the warehouse (Fig 2) provide a total of 57,000 slots for parts along 58 aisles (28 with racks on both sides, 30 with bin/facing rack combinations). Aisles are 6' (1.8 m) wide, with material extending 2' (5 cm) beyond each side of the bins or racks. Since vehicles are 5' (1.5 m) wide, they have only a 4" (10-cm) side clearance.

Guidance signals from computer to vehicles are conveyed along a grid of wires embedded in 5 mi (8 km) of slots diamond-sawed into the concrete floor of the warehouse. The computer routes each vehicle to the proper location along the grid and raises the picker cab to the proper elevation up to 20' (6.1 m) without rider action of any kind. Then the computer instructs the rider on a 192-character CRT which part to pick up or deposit. When the rider has carried out or tried to carry out the instructions, he enters the appropriate information through a control keyboard (Fig 3) on the vehicle by pressing either a single button to indicate "task complete" or several keys to specify and

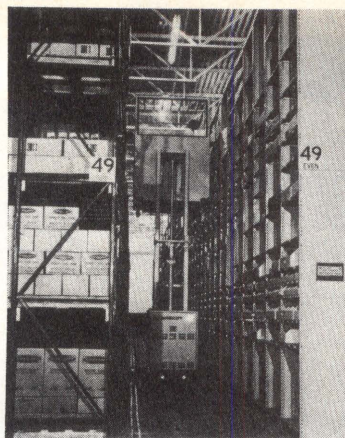


Fig 2 MHE vehicle. Under computer direction such units fill 500 orders a day—up to 4500 parts—from items stored in Mercury Marine warehouse. Wires embedded in warehouse concrete floor carry orders to and from computer and vehicle. Clearance of only 4" (10 cm) is maintained between racks and vehicles. Computer orders raise vehicle cab to proper height and instruct rider on vehicle CRT which parts to take from or add to storage module

identify an exception (such as part not in stock). This information is conveyed to the computer through the wires in the floor.

Each day the warehouse manager decides which vehicles to use for stocking, picking, or inventory checking and supplies this information to the warehouse control computer through the teletypewriter control console. Based on these directives, the computer communicates with the vehicles it will use.

To identify a vehicle's location to the warehouse control computer, its operator enters a pick aisle where a unique aisle code is embedded in the floor wires. The vehicle then transmits the code to the computer, giving location and direction of travel. This information is displayed by the computer on the vehicle CRT for operator confirmation via the keyboard. If everything agrees, the computer displays the run number and mode (pick or stock) in which the vehicle is to operate.

Once the operator has entered his number and that of the run, the computer specifies the storage module type the operator is to use. After that module is in place on the vehicle, the operator presses the "task complete" key and the computer automatically directs the vehicle to the first stop in the warehouse.

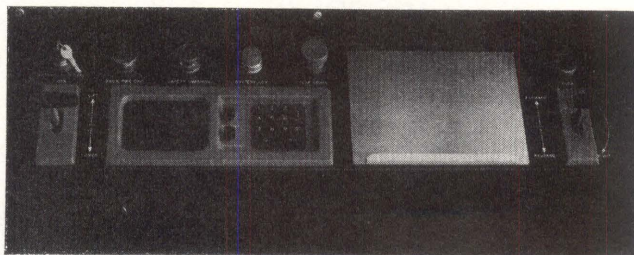


Fig 3 MHE vehicle control panel. Touch pad provides a combination of 13 numbers and functions, enabling operator to communicate with home base and to specify exception information (such as stock shortage). If picking, stocking, audit, or inventory instructions on CRT were performed as directed, operator presses "task compl" button above keyboard. Lift and steering controls are for offline use only. Brushed stainless steel area to right of keyboard is a writing surface in this configuration. However, an optional full alphanumeric label printer mounted at this location can print preselected fields of information from the CRT, freeing the operator of handwriting bag tags for small, unidentified parts

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The computer constantly polls vehicles to determine where they are and to make decisions on routes for each. If, for instance, another vehicle is operating in the aisle where the first stop is to be made, the computer guides the vehicle past that aisle to the next stop on the run, and returns it to the first stop later.

As the vehicle enters a clear aisle, the CRT displays the operator task to be performed. If the vehicle is picking, the display shows the part number, description, and quantity of the item to be picked; the location from which the parts are to be picked; and the position where the parts are to be put in the module. The vehicle automatically moves to the correct location and elevates the platform to the proper shelf.

On arrival at the appropriate location and level, the computer turns on a bin light which illuminates the proper side of the aisle and the bin. When the pick is complete, the operator presses the task complete button, and the warehouse control computer lowers the vehicle platform and moves the vehicle to the next location.

When the final pick is complete, the warehouse control computer directs the line printer in the computer room to print a packing slip for each order filled. At the vehicle's home location, the module is matched with the packing slip, demounted, and moved to the packing

line where packers check and pack the orders. Any back orders are noted both on the packing slip and, from a daily transaction tape generated by the warehouse control computer, reinstated on the central computer.

Comparable Installations

Computer-directed material handling systems of this type have also been installed in Oklahoma at Tinker Air Force Base near Oklahoma City, and at American Airlines Maintenance and Engineering Centers in Tulsa. Other systems are being installed at Outboard Marine Corp in Beloit, Wis; Kelly Air Force Base in San Antonio, Tex; and Raymond Corp, Mobility Systems' parent company.

The Tinker AFB installation covers 168,000 ft² (15,600 m²), comprising five storage segments of bin/shelf and rack configurations. Ten vehicles choose from 135,000 line items stored in 165,000 stock locations. An NCR Century 101 mainframe serves as the central computer and a Hewlett-Packard 2100A computer is the warehouse control unit.

In the American Airlines installation, a Century 201 mainframe interacts with an HP 2100A to access and maintain 116,000 parts. Thirty CRT/keyboard terminals in shop areas and warehouse are online to the mainframe to input shop requests. A pneumatic tube system included in this configuration enables a rush order to be entered, picked, packed into the tube, and delivered in less than 10 min.

The three systems under construction will be similar to those described above. However, each will include

We're showing off for Commonwealth Edison.

Chicago's Commonwealth Edison uses Ramtek color graphic displays for rapid display and status reporting of pipelines, valves, pumps, and other generating station data. A clear, color-coded display is updated every 5.0 seconds, giving near-instantaneous visual scan-log-alarm functions, bar graphs, one-line piping diagrams, flow status, etc.

Before the Ramtek systems were installed, status reporting was by hardwired mimic boards, black and white alphanumeric CRTs and typers.

The Ramtek system not only costs less, it also allows more information to be presented to the operator in a form that is quickly and easily under-

stood. This results in better operator efficiency, and faster alarm reaction time. In Commonwealth Edison's 16,000 Megawatt system, thirty Ramtek color graphics displays will be utilized.

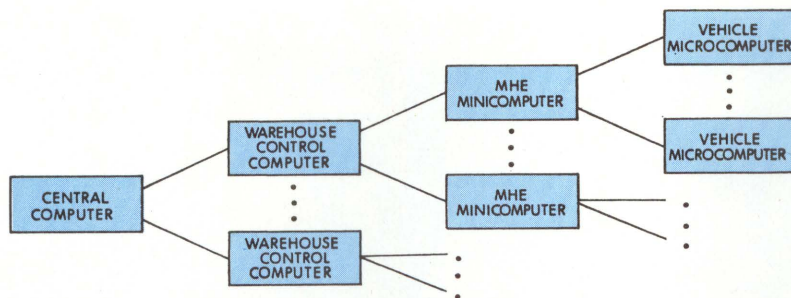


Fig 4 Control configuration of possible future installation. Balance of desired sophistication and ability to allocate capital funds is only limiting factor on scope of warehouse control systems. Central mainframe computer could feasibly be tied via sets of warehouse control and material handling equipment minicomputers to microcomputers which would control actual equipment

a Hewlett-Packard 21MX computer as warehouse control unit.

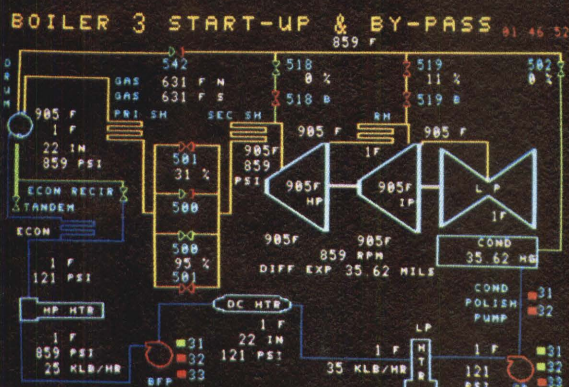
Possible Future Installations

Computer-controlled warehouse material handling systems can be as sophisticated as particular budgets and needs allow. A feasible extension of the present systems to a "total" system (Fig 4)* likely would include a central computer, one or more warehouse control computers, several material handling equip-

ment (MHE) minicomputers tied to each control computer, and a microcomputer on each of several vehicles directed by each of the MHE minicomputers.

The microcomputer would control actual functions of the vehicles but communicate via either wires or radio to the MHE minicomputer for directions. That

*B. Boldrin, "The Opportunities and Limitations of Automating Materials Handling Equipment," presented at National Plant Engineering, and Maintenance Conf, Chicago, Ill, May 12, 1977.



Commonwealth Edison monitors on-off, full-empty, flow status, and other parameters on a Ramtek FS-2400. Color is assigned for steam, water, no-flow, and oil flow to differentiate visually between materials and status. On the RM-9000, resolutions from 240 lines x 320 elements to 512 lines x 640 elements are available.

Commonwealth Edison is but one of a growing number of customers who are finding that Ramtek's raster scan modular graphics and imagery systems are giving them the expandability, flexibility, and increased productivity they need. Besides the basic alphanumeric and imaging capability, Ramtek offers a wide variety of other functions including graphics—vectors, conics, plots, bar charts—pseudocolor, and grey-scale translation.

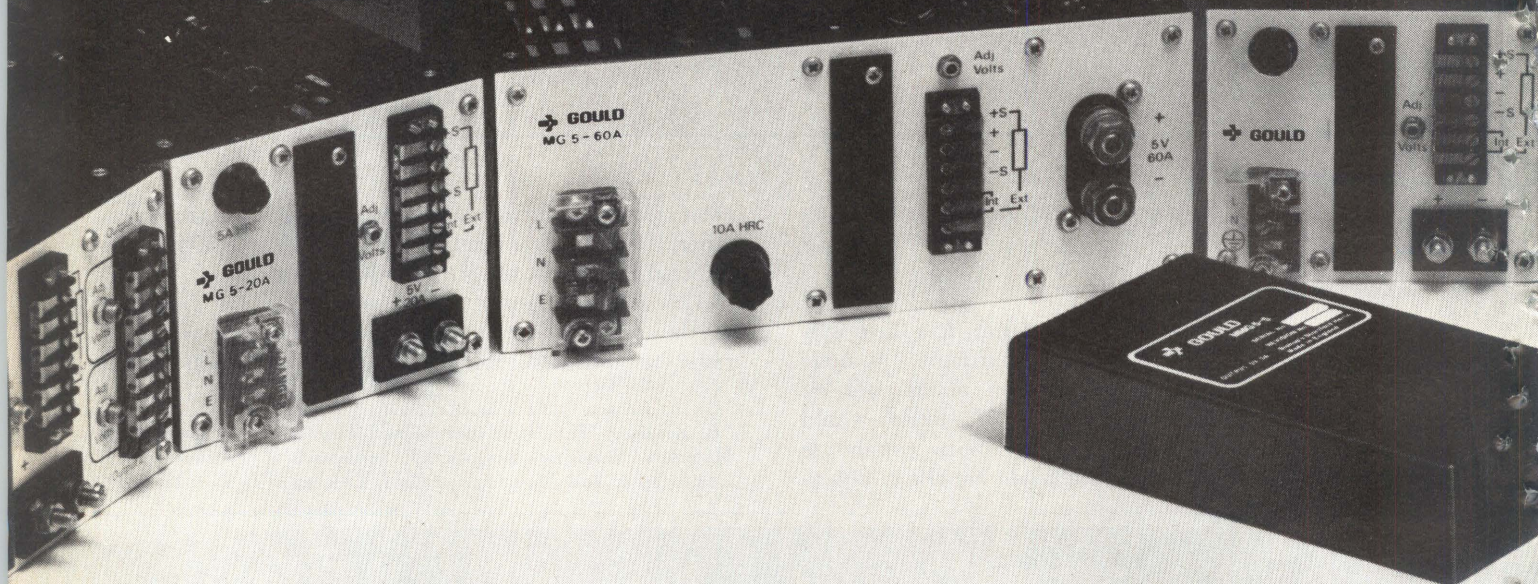
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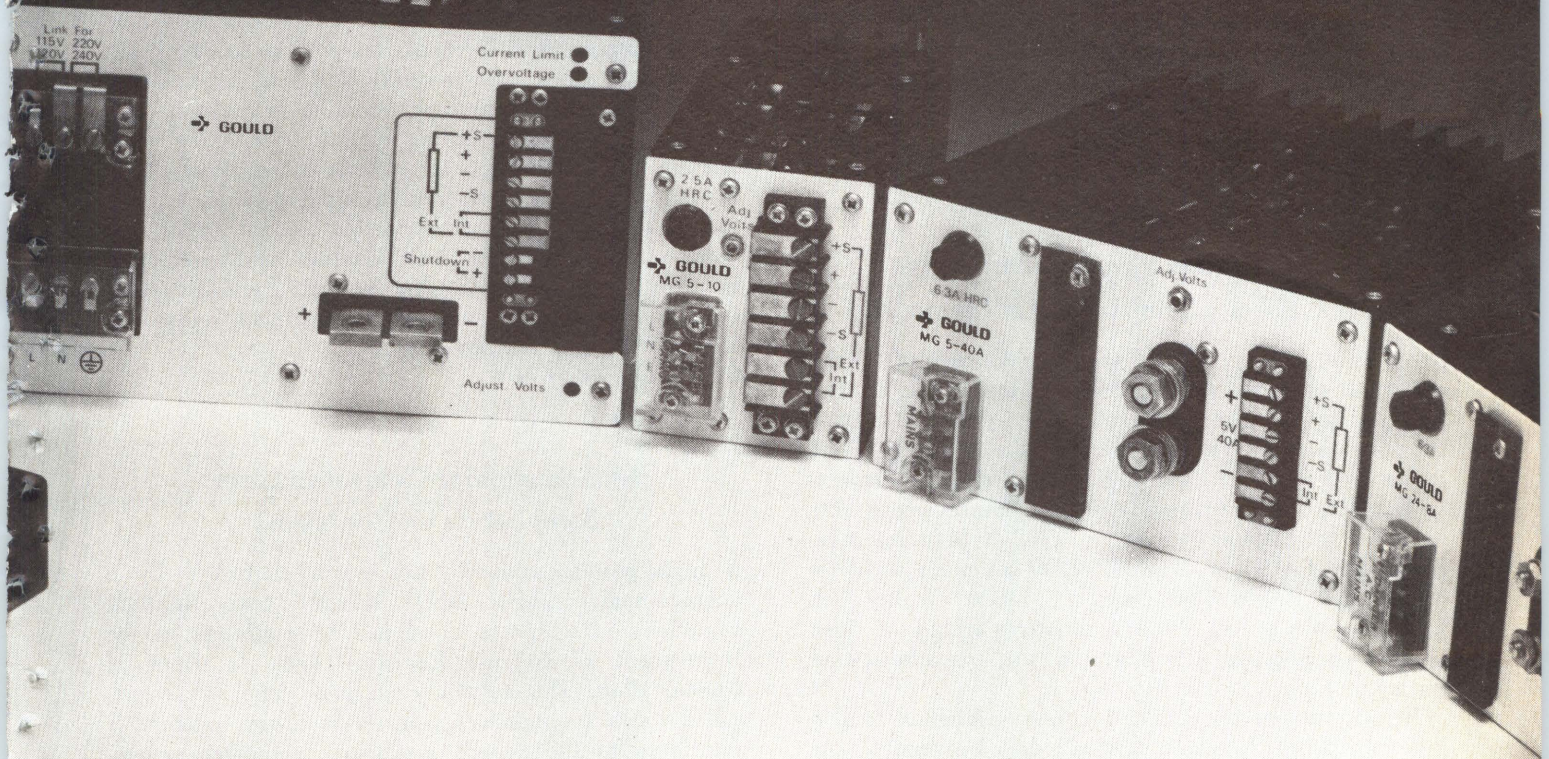
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CIRCLE 40 ON INQUIRY CARD

computer, in addition, would diagnose mechanical faults, maintain inventories, and keep track of MHE units.

Direction of MHE minicomputers would be handled by warehouse control computers which would carry a data base of all parts in the facility, direct order entries and receiving, produce management reports, and summarize activities for the central computer. That main-frame machine would direct all warehouse computers, maintain a corporate data base on all parts, permit online inquiries, and produce management reports on all corporate facilities.

Circle 160 on Inquiry Card

Weather Study System Incorporates High Capacity Semiconductor Memories

Research underway at Colorado State University toward achieving clear TV weather pictures makes use of two large scale semiconductor memory systems to back up the computer. An in-477, which stores and retrieves digital video image data, and five in-50 enhancement-table memories, to provide image improvement, are made by Intel Memory Systems, 1302 N Mathilda Ave, Sunnyvale, CA 94086. The HP 2100 computer was produced by Hewlett-Packard Co, 11000 Wolfe Rd, Cupertino, CA 95014. Other subsystems include a video overlay (512 x 512 x 8 bits), five D-A converters, and five TV monitors.

In this project on digital imaging—which is funded by the Army Research Office, the University, the National Science Foundation, and the National Aeronautics and Space Administration—the in-477 receives information from the computer and transmits it 16 times faster, using its shift register to attain a speed of 100 ns/word (10 MHz). It is a CRT refresh/special-purpose memory system with capacity up to 262k bits/card, available as a single- or multi-card memory for use with a 512 x 512-bit display matrix. The Colorado State University configuration has a maximum capacity of 16M bits and includes a built-in shift register on each of the 64 memory cards, a memory control, operation in single-bit and serial-bit modes, and a specially-designed enhancement lookup table using the in-50 memories. A complete 512-line refresh and update of the video display is provided in about 52 μ s (100 ns per picture element).

The memory permits data recall in various word lengths down to single bits. Scientists can work with partial dots, overlay dots on one another, and manipulate the picture data any number of ways. Each dot can be adjusted to one of 256 levels of lightness or darkness, permitting a wide range of contrast. More common techniques, such as rotating the image, photo-cropping on the monitor, and directing a pointer in the picture by digital control, are also used. High speed data output from the in-477 reaches the smaller, faster in-50 memories and acts as address input, caus-

ing the data to be relayed on from the in-50s in appropriately modified form (higher or lower contrast) and routed to the D-A converter and then on to the TV monitor.

Objectives of the research include new capabilities in image enhancement that may lead to many future improvements in weather study. These could include near-automatic weather maps, translating satellite data to superior video pictures with far less human data manipulation than at present; zooming in and magnifying a portion of the moving picture; combining color and black-and-white to etch details more clearly than present pictures, and tracing invisible weather features (such as hot air masses) as visible colored areas; and more accurate weather interpretation and prediction by airlines, airports, weather services, and scientists based on clearer TV pictures with greater knowledge of the earth's cloud formations.

Circle 161 on Inquiry Card

Microcomputer-Controlled Laser Burns Labels on Containers

A high powered pulsed laser beam controlled by a microcomputer burns labels directly onto shipping containers in a system developed by engineers at the Department of Defense Logistics Agency's depot in Ogden, Utah. The automatic package labeling system, called CAMS (container automatic marking system), is interfaced to the depot's mainframe computer system.

When shipping containers arrive to go through the laser marking system, all necessary data including sender, destination, weight, cube, and piece number are transferred from the depot mainframe computer to the laser microcomputer controlling CAMS. There digital data are transposed into a combination of digital and analog signals to control the modulation of the laser and the scanning of the optics to form the data printed on the containers.

A raster type scan forms the characters in a 5 x 7 dot matrix by letting the burn pass over seven times to make a complete line. As the beam impinges upon the surface in 2-mm dia bursts of 1000-W photon energy, a visible plume of flame several inches long flairs outward from each dot position. As the flame subsides the lettering appears. The system marks a package in an average of 12 s.

Penetration of the beam into the surface of the container is only superficial due to the high speed of the scan and short duration of the laser beam pulse. Recent tests, however, have shown that markings can also be "burned" directly onto coated metal surfaces by increasing the laser beam pulse. CAMS also contains a device which adds a color stripe to each package to indicate its shipping priority.

The marking chamber is made of PlexiglasTM which is optically opaque to the laser beam, allowing it to

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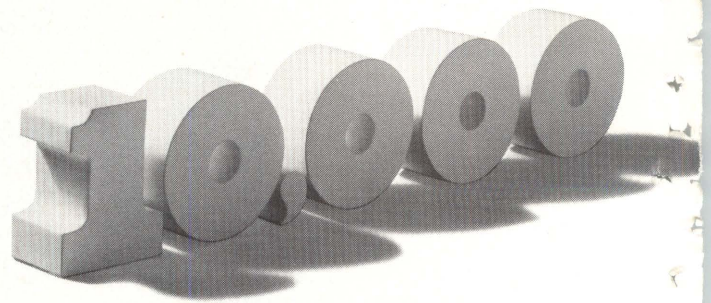
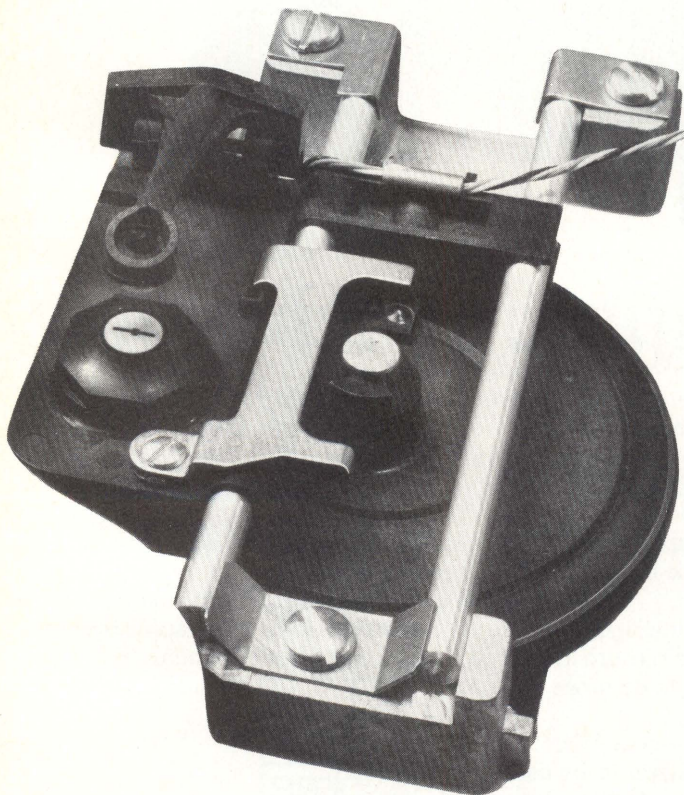
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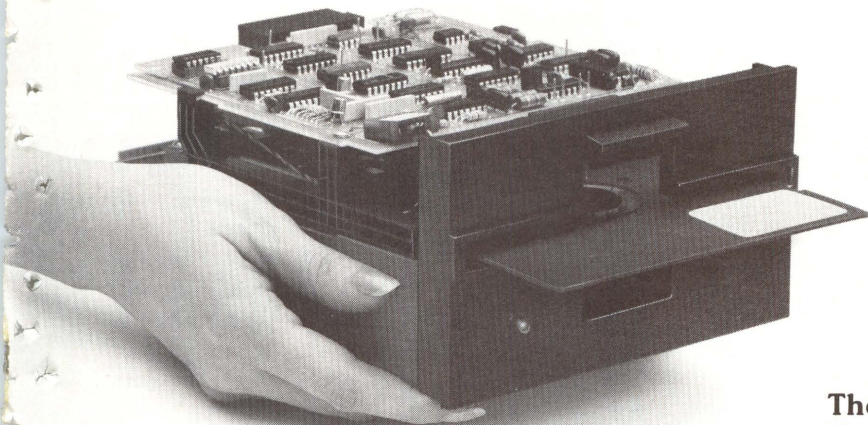
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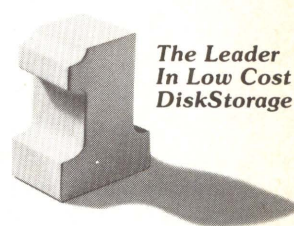
The SA4400 ministreaker controller controls up to three minifloppy drives, providing up to 241.8 kilobytes of on-line data storage. Using a modified IBM 3740 format and a 128 byte buffer, the controller operates on 8 bit byte bi-directional parallel I/O.

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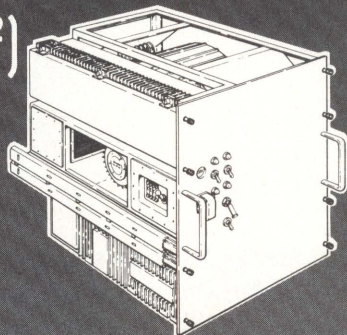
Which Major Navy Programs Specify Librascope's Mass Memory Subsystem?

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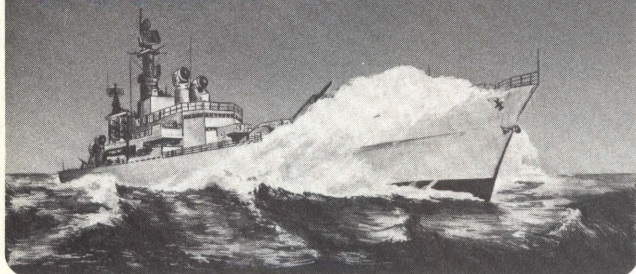
SURTASS

BQR-24



New one megaword Mass Memory Subsystem for TACINTEL features shock isolation and EMI/RFI secure packaging for mounting in an open standard 19" rack.

?



The answer? All of the above and many more. That's because more than 800 Series L107 or CL107 Mass Memory Subsystems in the field have logged remarkable records for reliability. Successful installations include not only shipboard, but also transportable hut, van and aircraft.

The militarized Mass Memory Subsystems will meet the environmental specifications of MIL-E-16400 and MIL-E-5400 including MIL-S-901C, the drop hammer shock test.

Interface is provided for computers such as the AN/UYK 7, 15 and 20 with NTDS fast I/O, and for the Rolm militarized computers.

For complete information call (213) 244-6541 or write to Librascope Division of the Singer Company, 833 Sonora Avenue, Glendale, California 91201.

SINGER
AEROSPACE & MARINE SYSTEMS

DIGITAL CONTROL AND AUTOMATION SYSTEMS

act as a safety enclosure but permitting visual inspection of the laser printing process. CAMS has been certified as environmentally safe by both OSHA and the Army Health Services Command.

Development costs, including breadboard models, software, hardware, installation, maintenance, and testing, totaled \$285,000. Costs for new systems in 1977 dollars are estimated at about \$94,000 each, \$80,000 of which is for hardware, installation, and maintenance equipment of the system. The remaining \$15,000 is for the materials handling equipment necessary to move the packages through the marking device.

The system is scheduled for extensive operational online test at Ogden after which a determination will be made whether or not to put it into operation at other depots. Because the system was conceived and developed by the Defense Logistics Agency, all patent rights are owned by the U.S. Government.

DC&AS BRIEF

CRT/Printer Terminals Enable Trucking Firm HQ-Depot Communications

Data communication between the Cherryville, NC headquarters of a major trucking firm and 63 freight terminals in the eastern U.S. is maintained over three 4800-baud and twelve 2400-baud circuits. VIP 7700 CRTs made by Honeywell Information Systems, 200 Smith St, Waltham, MA 02154 interface to a Honeywell model 6040 computer that has been upgraded to a series 60 dual-processor model 66/20. Local communication (one mile or less) is handled over the 4800-baud lines while long distance contacts are made over the 2400-baud circuits.

The system handles about 30,000 administrative-type messages and more than 35,000 transaction processing executive messages to update files each day. A total of 150 CRTs are used in the system, with more than 110 configured with receive-only printers. Each freight terminal uses a CRT configuration that can range from a single device with printer at the smaller terminals to as many as five devices with printers at the larger terminals.

CRT and printer buffer sizes are 1920 characters (one screen format). Each is separately addressable so a freight dispatcher can compose a message on the screen at the same time the printer is receiving a message. Printers operate at 30 char/s at the low volume locations and 120 char/s at higher volume sites. Usually one or two copies of a document are produced, but on freight bills one original and three copies are printed. □

The Datum Model 4091 Storage Module Disk Controller provides an interface between a Data General computer and the CDC storage module series or equivalent disk drive. The controller can accommodate from one to 2 drives in a single or dual processor environment. The controller contains a microprocessor that executes commands received from the Nova computer. It also generates and checks CRC characters and monitors for the detection of bad tracks. When one is encountered, it seeks automatically to an alternate track that was programmed during the format operation, without intervention from the operating software. With Datum-supplied RDOS-compatible software drivers, the Disk subsystem becomes an operational component of any Data General computer system.

New! DATUM Storage Module Controller

SYSTEM FEATURES

- Two sector Buffer eliminates a variety of I/O timing problems during computer-to-disk-to-computer operations
- Two sector numbering sequences permit variable data rate to the computer
- Automatic bad track detection and alternate track selection without operational software intervention
- Microprocessor for monitor and control of events
- Detached header complete with track status and a 16-bit CRC character
- Basic software compatibility with Data General's 4231 disk controller
- Programmable Error Recovery

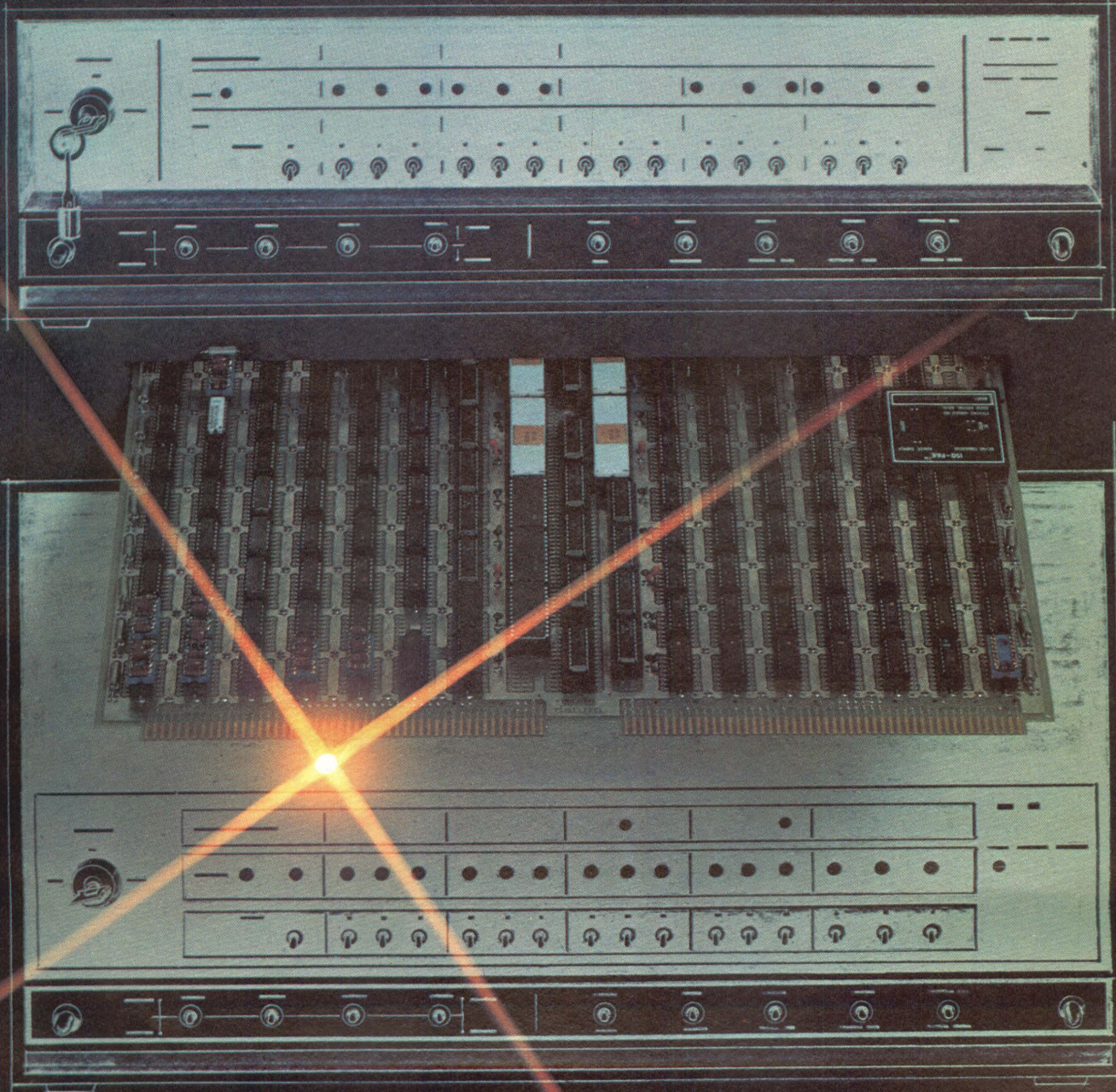
Peripheral Products Division

1363 S. State College Blvd.

Anaheim, California 92806

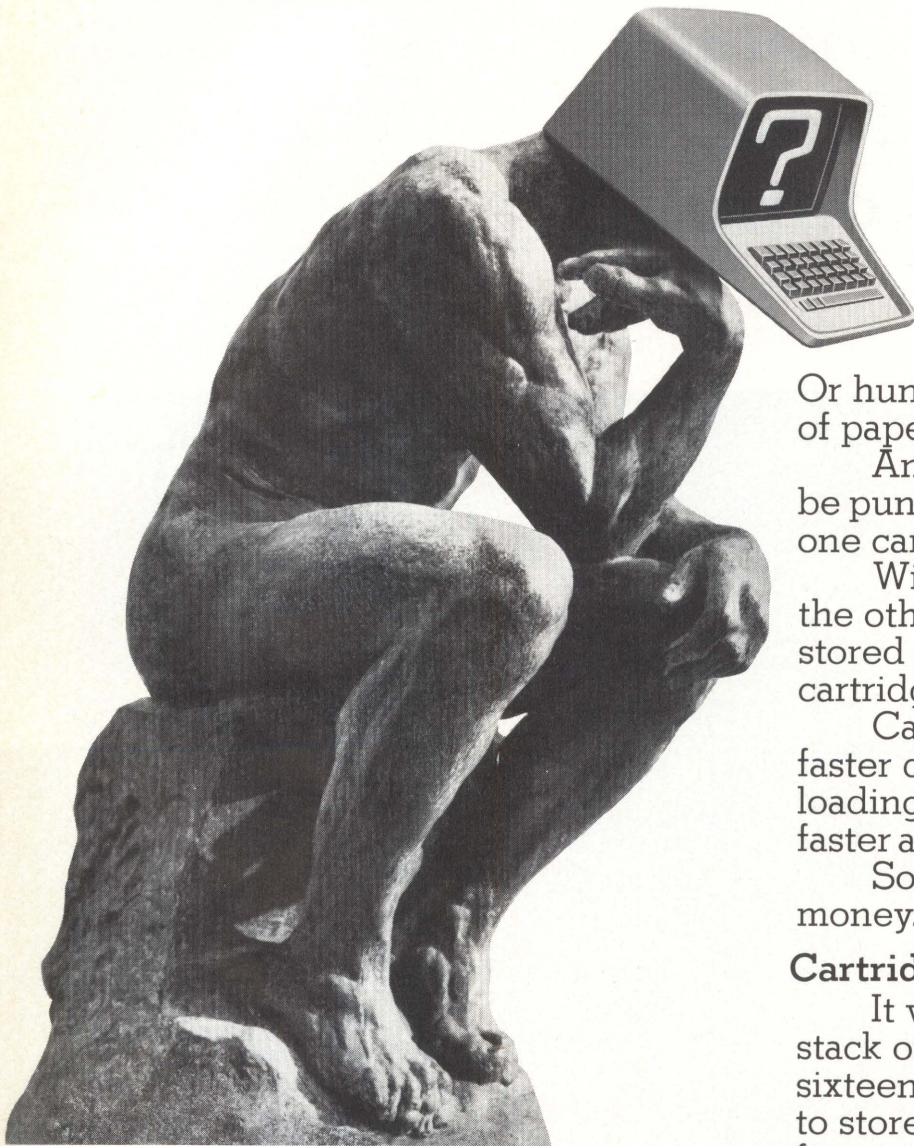
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Is your computer smart enough



One DC-300A cartridge equals almost 16 feet of cards.

Or hundreds of feet of paper tape.

And each program must be punched, verified and read one card at a time.

With our drive system, on the other hand, programs are stored on a single tape cartridge.

Cartridges offer much faster data storage, program loading, data transfer and faster access to the computer.

So you save time and money.

Cartridges take less space.

It would take a stack of cards almost sixteen feet high to store all the information you can store on a single 3MDC-300A data cartridge.

With cartridges, you can store all of your programs in a fraction of the space you'd need for cards or paper tape.

Your filing system is simplified and overhead is greatly reduced.

Cartridges won't fold, spindle or mutilate.

Unlike paper cards, you need never touch the media. It's well

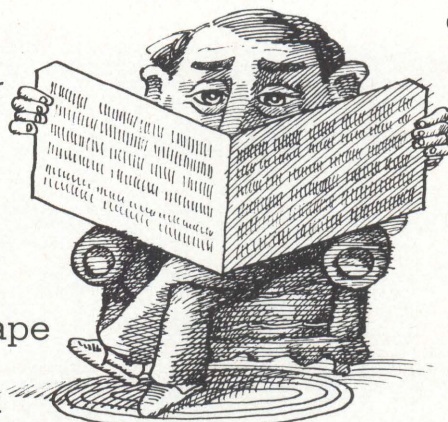
A 3M peripheral drive which uses 3M data cartridges is better than any drive which uses punched cards or paper tape.

And, if you'd take the time to ask it, your computer would probably tell you so.

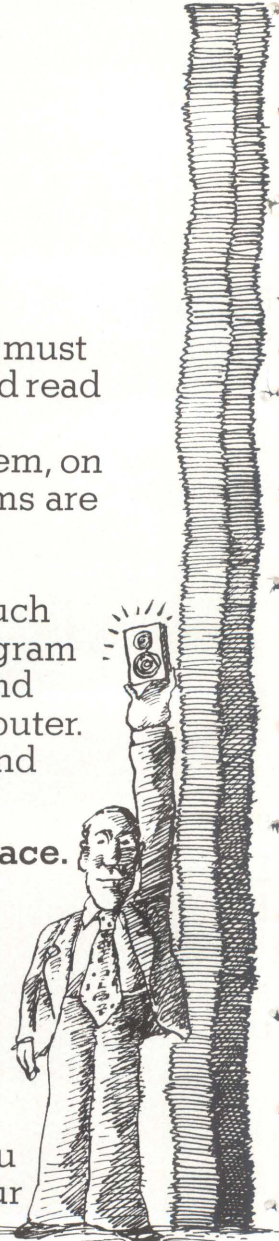
It's simple logic.

Cartridges are faster than cards.

Cards and paper tape are slow. It takes hundreds of cards for a single computer program.



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*One formatter can control
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Even if you
drop it, the program
will survive
unscathed.

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that the next
time you drop a
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Ask your computer to compare them
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we'll bet you will be.

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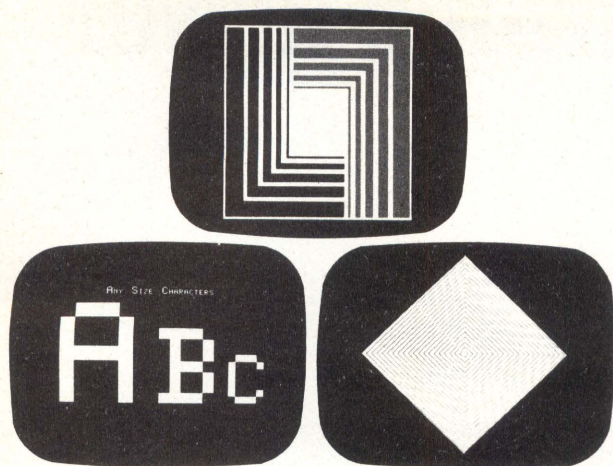
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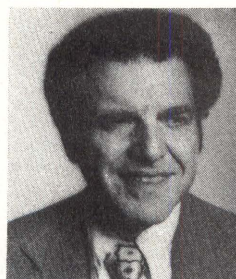


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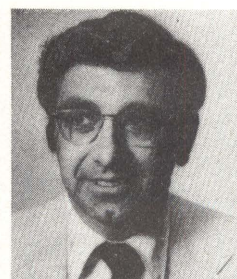
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MIDCON/77

November 8-10
Chicago, Illinois



David B. Pivan
Chairman of the Board



Richard H. Kruse
Program Chairman



Lewis H. Young
Keynote Speaker

Computer scientists, professionals, and manufacturers will convene in Chicago to participate in the first MIDCON electronic exposition and convention which features a 3-day professional program spotlighting applications, trends, advances, and directions of technology as they relate to the electronics field. Both exhibit and show will be co-sponsored by the regional and national elements of the Institute of Electrical and Electronics Engineers, and Electronic Representatives Association.

David B. Pivan (Pivan Management Co), chairman of the board, has coordinated the show and exhibit with the assistance of Richard H. Kruse (Martin Research), program chairman, who organized the 30 technical sessions presenting the viewpoints of consumers, users, designers, and manufacturers in relation to microcomputers, microprocessors, semiconductor memories, computer-aided design, microassemblers, and digital communications.

Special Activities

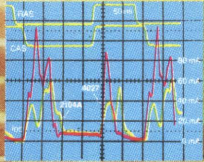
MIDCON has scheduled two events to highlight the conference and show. Designed for manufacturers, sales representatives, and electronics distributors, the MIDCON Marketing Workshop will preview the formal opening of the show on Monday, November 7. Three morning panels and discussion sessions will concentrate on the overall marketing pattern and how manufacturers, distributors, and sales reps fit into that

Intel delivers the only 16-pin 4K RAM that's sure to keep you smiling.

You may or may not think of your memory system as a masterpiece. But one thing is certain, once you've reached volume production you're going to be reluctant to make major changes. That's why it is so frustrating to find that a supplier has painted you into a corner by deciding to stop delivering the part you want. Or by trying to switch you to a newer, non-compatible part.

Smile. Our 2104A 16-pin 4K RAM is the answer. It's a direct replacement for both the older 4096 metal gate and newer 4027 silicon gate parts. The 2104A keeps your production line moving without expensive re-design. Plug it in and you're ready to go.

The 2104A is best for your new designs, too. We've been delivering this part in volume since July, 1976. So you can count on Intel to deliver the quantity you need, when you need it.



Delivery is not the only reason to specify the 2104A. There's not a 16-pin 4K RAM anywhere with lower power consumption. And because the 2104A has significantly lower current spikes

than other 16-pin 4K RAMs, there's less system noise. What it all means is that when you design your next system, it makes sense to design it using our 2104A.

	Maximum Access Time	Maximum Read/Write Cycle	Maximum I _{DD} Average
2104A-1	150 ns	320 ns	35 mA
2104A-2	200 ns	320 ns	32 mA
2104A-3	250 ns	375 ns	30 mA
2104A-4	300 ns	425 ns	30 mA
2104A	350 ns	500 ns	30 mA

You can order the 2104A from distributor stock. Contact: Almac/Stroum, Component Specialties, Cramer, Hamilton/Avnet, Industrial Components, Pioneer, Sheridan, Wyle/Elmar, Wyle/Liberty or L.A. Varah. Or write us. Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051.

In Europe, Telex 24814, Brussels.
In Japan, Telex 28426, Tokyo.

CIRCLE 47 ON INQUIRY CARD



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pattern. Also on Monday, Lewis H. Young, editor-in-chief of *Business Week* magazine and former editor of *Electronics*, will discuss the impact of new technology on the international economy in his keynote address to be delivered at the all-industry luncheon. Both events will be held at the Hyatt Regency O'Hare.

On the social side of the conference, an all-industry reception entitled "Octoberfest—A Harvest of Technology," featuring entertainment by a Tyrolean band, will take place in the Rosemont Ballroom of the Hyatt Regency O'Hare.

Exhibits

Products and systems of 200 manufacturers will be displayed at the O'Hare Exhibition Center in a 375-booth area covering production and packaging, components and microelectronics, instrument and control systems, and mini/micro computers and peripherals. Exhibit hours will be between 9:30 am and 6 pm, Tuesday and Thursday, November 8 and 10, and 9:30 am to 9 pm on Wednesday, November 9. In addition, a special energy exhibit consisting of a nuclear reactor display, a power management exhibit, and various approaches to solar energy systems will be presented by Argonne National Laboratory.

Registration

Registration for the show will take place at the O'Hare

Exhibition Center. A \$5 fee will cover all exhibits and professional sessions for three days.

Professional Program

Primary emphasis of the program will be to exchange ideas and experiences in an effort to provide solutions or alternatives to the problems that plague designers, engineers, and manufacturers. Presentations in the form of papers, tutorials, panel discussions, and seminars will cover a broad spectrum of subjects ranging from design techniques and considerations to applications and implementation of systems and components. The 30 half-day sessions will attempt to give attendees some insight into current problems and advancements in technology and the opportunity to compare similarities, differences, advantages, and disadvantages of certain products.

Five sessions will be held concurrently at 10 am and 2 pm on Tuesday, Wednesday, and Thursday in the Ballrooms of the Hyatt Regency O'Hare. Major areas of concentration will be microcomputers and peripherals, digital communications, microprocessors and LSI peripheral circuits, automatic test equipment, software design tools, LSI technology, computer-aided design, semiconductor memories, and markets such as home computing.

Only those sessions of particular interest to *Computer Design* readers are listed here. Information is necessarily limited to that available at press time.

MDB SYSTEMS presents... The NOVA* Connection

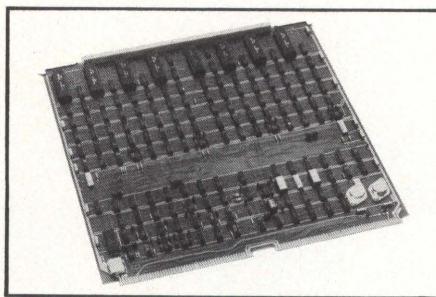
GP Interface Modules • Peripheral Controllers • Communications Interfaces • Accessory Hardware

New: Four or Eight Channel Multiplexors • Multiple I/O Controller

MDB Systems products always equal and usually exceed the host manufacturer's specifications and performance for a similar interface. MDB interfaces are software and diagnostic transparent to the host computer. MDB products are competitively priced; delivery is usually within 14 days ARO or sooner.

Here are some MDB Systems connections to Data General NOVA computers:

- ☐ General Purpose Interfaces: GPIO similar to Nova 4040, with PC'd interface logic and wire wrap section for 105 wire wrap devices. Full wire wrap board for 215



- sockets or DIP devices.
- ☐ Device Controllers for most major manufacturer's Printers Card equipment Paper Tape equipment
- ☐ Four or eight channel Multiplexors, Nova 4060 compatible, with many additional program controlled features. Full modem control contained on board. Optional panel for multiplexor provides standard 25 pin communications connectors for each channel.

- ☐ Multiple I/O board for TTY and/or RS-232 Controllers. Options include Real Time Clock and modem control.

- ☐ Accessory Hardware Front loading expansion chassis, optional power supply configurations, chassis may be terminated or daisy chained.

Terminator modules.

Extender boards.

Check first with MDB Systems for your NOVA computer interface requirements.

MDB also supplies interface modules for DEC PDP-11* and Interdata computers and for DEC's LSI-11 microprocessor.

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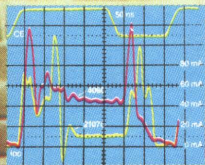
*TMs Data General Corp. & Digital Equipment Corp.

CIRCLE 48 FOR NOVA; 49 FOR PDP-11; 50 FOR INTERDATA; 51 FOR LSI-11.

Intel delivers a better 22-pin 4K RAM for people who are never quite satisfied.

For some people "good enough" is never quite good enough. In 1972 we introduced the industry's first 22-pin 4K RAM, the 2107. But we weren't content to stop there. So we followed with the 2107A. Then in 1975 the 2107B. Now, introducing the 2107C. Compare it with any 4K dynamic RAM. The results are sure to put a smile on your face.

The 2107C delivers a new standard of performance. Access time: 150 ns. Power consumption: 40% lower than the TMS 4060 or our own 2107B. Current spikes: significantly lower than competitor's parts means less system noise with the 2107C. Supply tolerance: $\pm 10\%$ in all power supplies gives you the widest system operating margins available anywhere.



Best of all, the 2107C is already in volume production and available in both hermetic and plastic packages. Plan now to upgrade your systems now using our 2107B or any of its second sources. For a complimentary P2107C evaluation sample and data sheet,

	2107C-1	2107C-2	2107C
Maximum Access Time	150 ns	200 ns	250 ns
Maximum Read/Write Cycle	380 ns	400 ns	430 ns
Maximum I _{DD} Average	35 mA	33 mA	30 mA
Power Supply Tolerance	$\pm 10\%$	$\pm 10\%$	$\pm 10\%$

contact your Intel sales office. To order, contact Almac/Stroum, Component Specialties, Cramer, Hamilton/Avnet, Industrial Components, Pioneer, Sheridan, Wyle/Elmar, Wyle/Liberty or L.A. Varah. Or write us. Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051.

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Sessions at a Glance

TUESDAY		WEDNESDAY		THURSDAY	
10:00 am	2:00 pm	10:00 am	2:00 pm	10:00 am	2:00 pm
<p>1</p> <p>Automated Software Design Tools</p> <p>Peter Weiner Interactive System Corp</p>	<p>6</p> <p>Software Engineering Tools</p> <p>Chong Lee Tektronix</p>	<p>11</p> <p>Microassemblers: A Prototyping Tool for Bit-Slice Designs</p> <p>Stephen Y. Lau Signetics</p>	<p>16</p> <p>Architectural Trends in Micro-Based Computer Systems</p> <p>Al Reszka Teletype Corp</p>	<p>21</p> <p>New Aids for Designing With Microprocessors</p> <p>Bill Furlow Tektronix</p>	<p>26</p> <p>Home Computers: Next Billion Dollar Market?</p> <p>Frank Burge Regis McKenna</p>
<p>2</p> <p>Update on Minimum Chip Microcomputer Systems</p> <p>Alan Weissberger Signetics</p>	<p>7</p> <p>Microcomputer Systems for Under \$10</p> <p>Frank Burge Regis McKenna</p>	<p>12</p> <p>Microprocessors: Interfacing With the Outside World (I)</p> <p>Robert Walker Intel Corp</p>	<p>17</p> <p>Microprocessors: Interfacing With the Outside World (II)</p> <p>Andy Santoni Electronic Design</p>	<p>22</p> <p>Microprocessors: Interfacing With the Outside World (III)</p> <p>K.N. Sundaram Signetics</p>	<p>27</p> <p>Minicomputer and Microcomputer Applications</p> <p>Fred Lesh Jet Propulsion Laboratory</p>
	<p>8</p> <p>Product Liability: Domestic and International Implications</p> <p>Andy Santoni Electronic Design</p>	<p>14</p> <p>Digital Communications: Hardware, Analysis, and Design</p> <p>John H. Park University of Minnesota</p>	<p>18</p> <p>Industrial Process Control; Applications of Electronics</p> <p>Alfred Watson Westinghouse Electric</p>	<p>24</p> <p>CAD: Applications and Techniques</p> <p>George Zobrist University of Toledo</p>	<p>29</p> <p>New Developments in Semiconductor Memories</p> <p>Steve Jasper Signetics</p>
			<p>20</p> <p>New Techniques in Automatic Testing</p> <p>Gerald Kutcher Inforex, Inc</p>	<p>25</p> <p>Analog Circuit Board Fault Diagnosis</p> <p>Michael W. Salter GenRad, Inc</p>	<p>30</p> <p>Fault Isolation of Analog PCBs</p> <p>Ravi Shah Martin Marietta Corp</p>

**Ramtek's new
MICROGRAPHIC™ terminal
gives you color, intelligence,
graphics, and
alphanumerics at a price
you can afford.**



Color and smarts don't cost a lot anymore.

Here's great resolution and a bright, flicker-free display on a matrix of 512 elements by 256 lines in a terminal that's easy to program to your requirements.

No longer do you have to put up with poor resolution in economy-priced terminals. Ramtek gives you a combination of true graphics—such as vectors, conics, plots and bar charts—and high-speed alphanumerics with a high-resolution industrial-quality monitor. You can choose two sets of 8 colors for both graphics and alphanumerics. Dual and split screen capability too, with all the price/performance benefits of raster scan technology. And the independent alphanumeric refresh offers you single-character addressability within a visible matrix of 25 rows of 80 characters that are bright, crisp, sharp, and well defined. The refresh memory also allows selective erase, modification, and update.

The MICROGRAPHIC terminal is controlled by a powerful Z-80 microprocessor with up to 28K bytes of PROM and 16K bytes of RAM. Ramtek's control software gives you TTY compatibility and high-level graphic functions commanded by ASCII text strings. Choose from an extensive list of options such as additional serial I/O ports, alphanumeric overlays, programmable fonts, and packaged software.

Best of all, you'll find Ramtek gives you an affordable price, depending upon your individual requirements. Find out more by contacting us. We're Ramtek, 585 N. Mary Avenue, Sunnyvale CA 94086. In a hurry? Pick up the phone and call us. We'll tell you why you can afford color and smarts.

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The heart of our 3040A is a new merged sequence technique which lets you mix your test codes with automatically-generated sequences. And the best simulator around: your own known-good board. And dynamic LSI/fault isolation, automatic, manual or both!

Fluke hasn't forgotten about the bad boards either. After the tester nails the bad ones, we automate the troubleshooting. Our Autotrack™ computer-guided troubleshooting leads the operator to the fault. With the new 3041A programming station, you describe the board onto a floppy disk and the 3040A does the rest.

The 3040A, with up to 240-pin capability, is \$60,000 to \$95,000*, de-

pending on option configuration.

The 3020A logic test system, at about \$32,000*, is perfect for production test of all popular logic families.

For light production test or field service, our model 3010A has 128-pin capability for under \$15,000*.

Call (415) 965-0350, collect. Ask for the complete story on our high-ranking Logictester™ family, or the location of the closest Fluke office. Or, write: Fluke Trendar, a subsidiary of John Fluke Mfg. Co., Inc., 630 Clyde Ave., Mountain View, CA 94043.

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*U.S. price only.

Command Performance: Demand Fluke Logic Test.

For literature, circle 54 on Inquiry Card. For a demonstration, circle 55 on Inquiry Card.



Changes in design approaches to communications systems have allowed microcomputers to distribute processing functions throughout the network, with trunk-line capacity savings, increased throughput, minimal delays, and low cost system elements

Microcomputers Decentralize Processing in Data Communications Network

Donald J. Mueller

**Computer Transmission Corporation
El Segundo, California**

A modern data communications system provides many value-added capabilities to the user, such as error control, data concentration and switching, centralized network management, and centralized diagnostics, which require a large measure of data processing power within the network. Two basic design approaches that can provide this processing power are to centralize processing in a small number of network nodes and use high performance minicomputers, or to distribute processing power throughout the network using microcomputers in all or most network nodes for processing locally.

In the centralized approach, the advantages are theoretically less expense because a processor is shared among many nodes, and easier management because of the centralized nature (software changes, etc). Disadvantages are the placing of a heavy processing load on the minicomputer which causes processes to slow down during busy periods, much overhead data which must be passed on the trunk lines to remote nodes, and network vulnerability. If the centralized processor should fail, many users would lose service. If a trunk line should fail or have a high error rate, the processes for the remote node would be stopped or severely slowed down.

Distributing the processes with a microcomputer in all network nodes eliminates the disadvantages of the centralized approach. Management of software changes can be accomplished by storing a large part of the microcomputer program in random-access memory (RAM), which may be downline loaded from the minicomputer. Programmable read-only memory (p/ROM) is used to

store an auto-load function for the downline load. The extra cost associated with the microcomputer approach is offset by the ability to decrease the number of large centralized nodes because of the reduced processing demands. A brief description of the M3200* network switching and management system¹ and architecture of the system elements is included with a comprehensive discussion of design features and applications of an 8080A microprocessor-based microcomputer to network processes.

Network System Description

An advanced packet and circuit switching and management system, the M3200 networks consist of a family of data switches and multiplexers interconnected by trunk facilities. This system has minicomputer-based large switching nodes and microcomputer-based small switching nodes, each of which performs a variety of signal and data processing on the bus system in a multiprocessor environment. Processing includes packet (division of data into small, dynamically routed blocks with error control) and circuit switching, network partitioning (many user groups on the same network, with each group containing its own private subnetwork), error control, data concentration (elimination of redundant information),

*A trademark of Computer Transmission Corp, El Segundo, Calif.

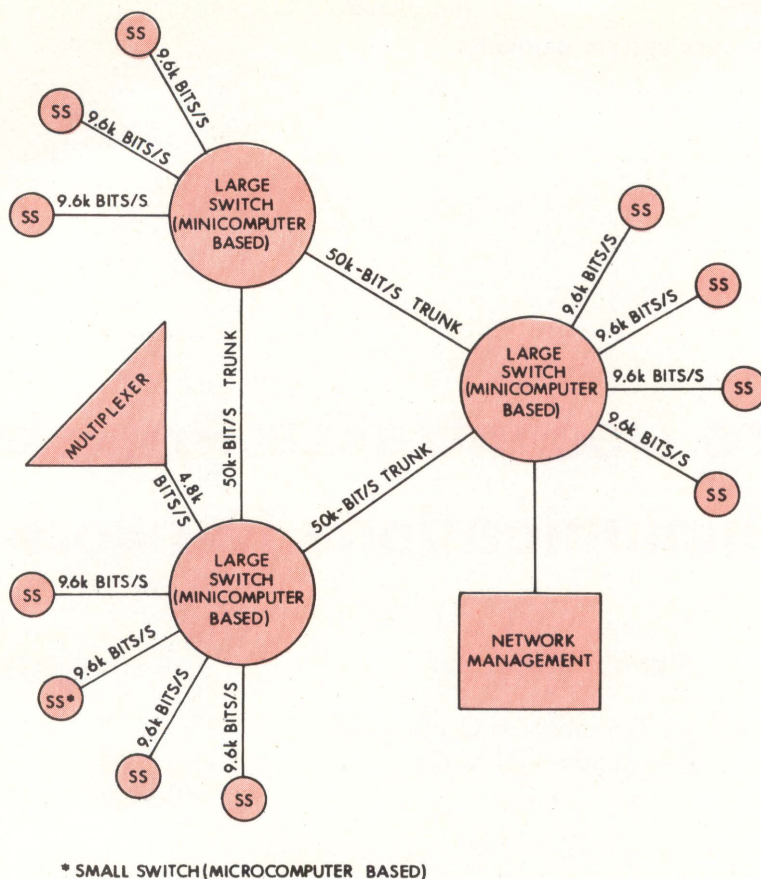


Fig 1 Typical network. Sample M3200 network illustrates relationship of various network elements. Large switches service major nodes and interconnect with high speed 50k-bit/s trunk lines. Small switches service outlying nodes and connect to one large switch over 9.6k-bit/s trunks. One major node has network management system connected to large switch

optimal use of trunk-line capacity, and centralized network control and diagnostics.

A network might be constructed as in Fig 1. The large switches and network management system are minicomputer-based while the small switches and multiplexers are microcomputer-based. In this organization, all network configuration and diagnostic control information flows outward from the network manager to the minicomputers and then to the microcomputers. Diagnostic and status reports are passed from the micro and minicomputers to the network manager. Since processes are performed locally at each switch and multiplexer, very little management data are passed over trunk lines—only commands to start certain processes and the result of these processes.

Switch Process Orientation

The Pacuit** (packet/circuit) switch may be viewed as a processing system under control of a switch control program which uses an operating system, applications software, and hardwired devices to create processes associated with network control.² Fig 2 shows a simplified overview of the processes within a switch. Conceivably, all these major processes, and the hundreds of associated smaller ones, could be mechanized in a large general-

purpose computing system. Basic switching processes, however, must be done in real time, and throughput and delay constraints required for the system usually demand that certain bit- and character-oriented processes be performed with hardwired devices or fast dedicated microprocessors. Slower management and control processes can be performed in undedicated, slower processors.

Each of the major processes calls upon a multitude of smaller ones. This is especially true of management processes. Resource allocation, for example, includes trunk capacity allocation, whose management is implemented by a complex series of discrete commands given to the hardwired trunk interface processor. If a single minicomputer were performing all the management tasks, the system would not be responsive enough because of the many detailed operations which must be done for each task. Hence, the need arises for a type of multiprocessor approach to perform some of the management tasks. For this reason, a microcomputer was developed, based on the 8080A processor which is well documented, has a large base of support software, is readily available from several manufacturers, is inexpensive, and has a processing speed, 8-bit byte, and instruction set that

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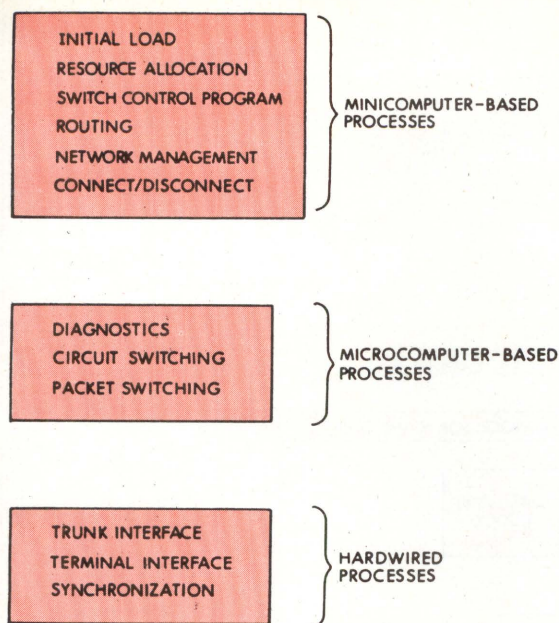


Fig 2 Major processes within data switch. Initial load, resource allocation, switch control program, routing, network management, and connect/disconnect processes are mechanized in minicomputer. Diagnostics are mechanized in microcomputer; circuit switching and packet processing in fast bipolar processors; and trunk interface, terminal interface, and synchronization processes in hardwired processors

match those required to perform several management tasks.

Microcomputer Architecture

Having selected the microprocessor for the microcomputer, the system integrating requirements included how to optimize the processing power of the processor, use an 8-bit processor effectively in a 16-bit environment, interface a slow metal-oxide semiconductor (MOS) device to a fast bipolar bus to prevent bus performance from deteriorating, supplement the processor capabilities to make it more useful in a network system environment, and interface the microcomputer to the bus so that a variety of tasks could be performed.

The basic microcomputer architecture and an added capability version are shown in Fig 3. The microprocessor is used as the main processing element. Fixed microcomputer programs (bootstrap load, utility subroutines, etc) are stored in a p/ROM, whose size varies in accordance with the application. Initially providing a means of storing downline loadable program and temporary data, the RAM is also used as a buffer for communicating with the bus system.

An 8-bit stack pointer addresses the RAM and is used for storing requests from the bus which create interrupts

to the processor. If the interrupts are locked out, data transactions continue to take place and data defining the type of transaction are stored on the stack. The stack pointer increments automatically after it has stored information in a location.

Connected to the light emitting diodes (LEDs) on the front panel is a 4-bit display register capable of being loaded from the microprocessor. The display has various meanings depending on the application. A real-time clock provides the capabilities of timing events, interrupting the microcomputer at the end of a programmed time interval.

A dual-processor microcomputer (using an 8080A for each processor) was designed primarily to mechanize the small switch system, which requires blocks of data to be transmitted using a synchronous data link control (SDLC) format to the large switch. To improve throughput of the processor, data characters are taken out of a dual-port community RAM direct memory access (DMA) processor and converted to SDLC format by the SDLC processors.

The dual-port RAM is used for interprocess communication between processors and may be accessed by each. In case of conflicts between processors over use of memory, access requests are handled on a first come, first served basis. If both processors simultaneously request memory, processor A is given priority. Software techniques have been developed to reduce such conflicts.

Small Switch Processing

In Fig 1 the small switches at the remote nodes perform data concentration, error control, and switching. Since trunk lines going out to these switches are limited to a 9.6-bit/s data rate, it is feasible for a microcomputer to carry out these processes. However, higher level control functions, such as network partitioning, diagnostic control, and circuit routing, are controlled by the large switch, primarily because of the large memory required to store channel and network parameters. The small switch is slaved to the large switch and performs data concentration, error control, and switching processes only on channels defined by the large switch.

The microcomputer in the small switch must scan all connected channels for data characters and all nonconnected channels for a bid for service (ie, ring indicator), and pack the significant data or control bytes into a format suitable for transmission to the large switch. If a channel is to be switched locally (ie, not transmitted to a large switch), the microcomputer simply delivers the data to the proper local channel.

After packing data and control characters into a concentrated frame, the microcomputer mechanizes an automatic retransmission request (ARQ) protocol with the large switch. This involves assigning sequence numbers to a frame of data, calculating a frame check sequence (FCS), transmitting the frame of data, and storing it in local memory for possible retransmission until an acknowledgement (ACK) for this frame has been received from the large switch. The reverse procedure must take place for frames of data received from the large switch.

In the small switch application, the microprocessor's speed is the major limiting factor to processing data. To overcome this, three enhancements have been made to the

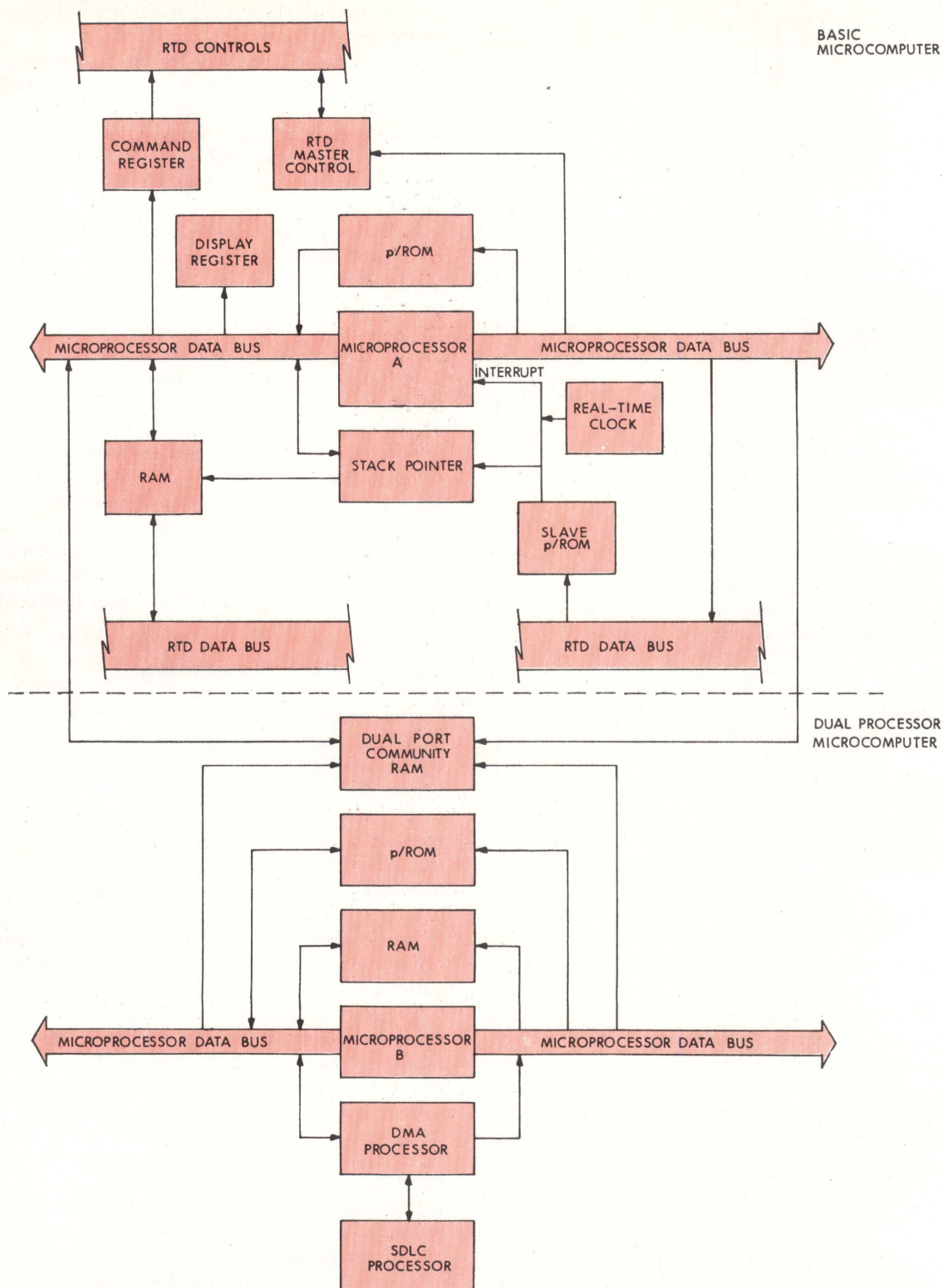


Fig 3 Basic microcomputer. Main building blocks of basic microcomputer include 8080A microprocessor; p/ROM for program storage; RAM for program storage, data storage, and bus I/O; stack pointer to address RAM and store RTD bus requests which cause interrupts to processor; display register; and real-time clock. Dual-processor version is available which adds another 8080A processor with its own RAM and p/ROM, special DMA processor, SDLC processor, and dual-port community memory

original microcomputer design. A 250-ns microcycle 8080A has been substituted for the old 500-ns 8080A, a second 8080A has been added to the microcomputer module to divide the processing load, and external hardware has been added to do some of the bit processing required by the ARQ technique.

Community Memory

Small switch processing tasks are easily divisible. Scanning and frame construction processes are separable from the ARQ process with the second 8080A handling the ARQ processing; however, data must be passed from the first microprocessor to the second. A dual-port community memory system effectively mechanizes the communications path.

The first microprocessor simply builds blocks of data (which it must do anyway) in the community memory while the second one controls the movement of data blocks through the DMA and SDLC processors. In this way, no special input/output (I/O) is required for inter-processor communications using normal memory access instructions.

Dual-port memory hardware gives access to the first processor requesting it. If the processors request access simultaneously, processor A is given access and processor

B must wait. If the processors were transferring large blocks of data into and out of the community memory simultaneously, there would be many chances for contention for memory access, resulting in each processor being slowed down while waiting for the other to complete an access. To avoid this, the software is written to require that each processor make the other aware of when it needs to access the community memory for a large data transfer. The other processor then waits until the first one has completed its data transfer. During the wait period, other processes are done in private RAM.

The ARQ process requires considerable bit-by-bit manipulation to calculate the FCS. While very efficient in handling 8-bit bytes, the microprocessor is inefficient for bit-by-bit processing that requires a lot of shifting (most general-purpose microprocessors share this same weakness). Therefore, the FCS has been mechanized in hardware external to the microprocessor; it can deliver 8-bit data to the hardware, which can then perform the shifting process and FCS calculations.

System Bus Structure

The bus structure of the network system is designed to handle the following requirements prevailing in a communication switch environment: a large number of I/O

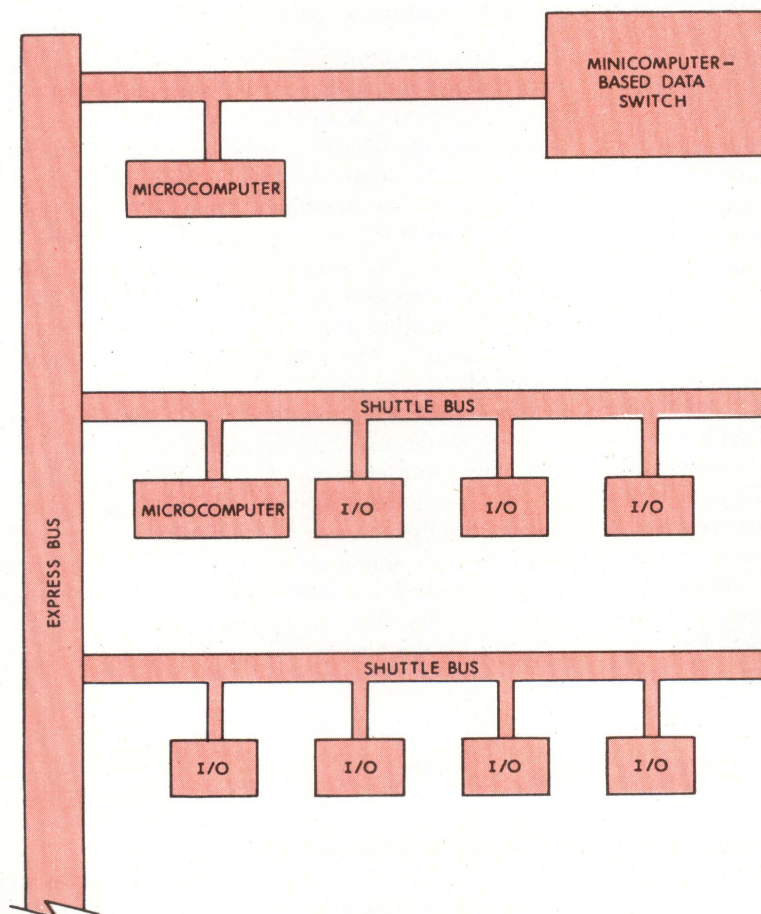


Fig 4 Bus system communication. RTD bus system uses master/slave protocol for communicating. Master device presents command and address to slave device; data transfer between master and slave then takes place. Device on any shuttle bus can address any other device on any bus. Concurrent bus transactions can be performed on shuttle buses unless they require express bus. Device can take control of shuttle bus by requesting its use and by being notified by bus controller of its master status. Top shuttle bus in RTD bus system consists of special microcomputer-based interface to minicomputer-based data switch. Microcomputer resident on the shuttle bus (up to eight microcomputers/shuttle bus) is dedicated to background tasks

devices, namely, the communication channels; a variety of speed and throughput devices on the bus, due to the requirement for handling a number of different communication channels; high throughput of the system because a switch is useful only when handling a large number of channels; a bus which may have a community memory accessed by different processors to perform the switching; and a high degree of processing power due to increasing demands on the communication networks to provide new facilities. To satisfy these requirements, a multibus, multiprocessor system has been devised. The bus structure, as shown in Fig 4, is called the RTD (real-time device) bus system. This bus structure is divided into two major buses: an express bus and a shuttle bus. The high throughput express bus connects all shuttle buses.

RTD Bus Interface

To utilize eight bits effectively in a 16-bit environment and to minimize processing time associated with input and output, an RTD bus interface was developed to augment the microprocessor. The RTD bus is a 16-address, 16-data, and 4-command bit bus. Data input and output are done in a DMA mode to RAM. RAM is organized so that it appears to be either eight or 16 bits. To the microprocessor it appears to be an 8-bit memory which can be addressed through normal addressing modes; when accessed from the RTD bus, the RAM appears to be 16 bits, as shown in Fig 5.

Microprocessor programs interact with other devices on the bus in two ways, either by acquiring control of the bus (becoming the bus master) and addressing another device on the bus for a bus transaction, or by responding to a request by another master on the bus and thus becoming a slave to the requesting device. Since all microcomputers on the bus communicate in these two modes, any processor can communicate with any number of other processors without conflict. Control over the tasks of another module is achieved by setting flags in predefined locations in that module.

Bus Master and Slave Operation

A microprocessor can give a bus master command simply by issuing a memory write command with specified address and data bits. Since the microprocessor has only eight data bits, a means of providing 16 data bits must be supplied. RAM locations 0 to 16 are reserved for communication to the RTD bus. When a memory write command is issued, with the most significant address bit set, 16 address bits and eight data bits are presented on the microprocessor address and data buses. These bits are given specific meaning for the duration of the bus command. Eight data bits are used to address the RAM and select a 16-bit location for presentation to the bus. DMA is done at the specified address to store/retrieve the bus data. The bus address bits are defined by the 15 least significant microprocessor address bits and by the most significant data bit. The bus command register must be loaded in advance of the actual bus command by an OUT command. To execute a bus command, the software must load bus data in RAM, load bus command register with an OUT command, and perform a memory

access command (such as MOV M, A) with the microprocessor address and data lines as specified previously (Fig 6).

Another device on the RTD bus can address the microprocessor, in which case it acts as a slave and an interrupt is generated. Bus conditions that cause an interrupt are decided by a slave p/ROM (s-p/ROM) organized as 512 x 8 bits. It is addressed by bus command and address control bits. The action to be taken under different bus conditions is determined by the following commands programmable through this s-p/ROM.

Interrupt Vector—There are seven possible vector addresses that the microprocessor jumps to when a command is received. Three bits select the interrupt address for given command and address bits that form the address field. If the interrupt is not desired, the interrupt vector field is set to zero.

Input/Output—By setting a bit, a command can be defined to be an input to or an output from the microcomputer. Thus, a command can be interpreted in many ways, depending upon the particular usage of the microcomputer.

Address Selection—Commands to the microcomputer by a master device are steered to RAM on a DMA basis by address logic. Address selection logic forms a 10-bit address from a combination of command and address bits specified by the master device. Eight different combinations of bits can be selected. Address and command fields are partitioned in such a manner that, by intelligent selection of these bits, data can be steered to many different locations in RAM.

A slave operation takes place as follows. Upon receiving a command with a nonzero s-p/ROM output, the 16-bit RAM address is stored in a location specified by the stack register, which is an 8-bit register loaded by the processor. It points to the location in RAM where the RTD address, as generated from s-p/ROM mapping, is stored. The stack is incremented after every slave operation. Thus, by setting the register to a desired value, the microprocessor can go through several slave cycles without spending any processing time. The stack pointer can be read to find out how many bus operations have taken place.

Stacking bus transactions and accessing memory in a DMA mode for bus data are important tasks in a multiprocessor environment. Processors can get on and off the bus quickly because the slave processor can respond rapidly. If a burst of different bus transactions are directed at a single slave processor, they are responded to and stacked for later processing. Without this stacking capability, the entire bus system could slow down waiting for the busy processor to respond to transactions.

p/ROM Power Reduction

High speed p/ROMs are readily available at cost-effective prices; one problem with them, however, is the power consumption required for a large memory. The microcomputer has a 16k x 8-bit p/ROM. If p/ROMs were used directly, they would draw 6.4 A from a 5-V power supply.

Several alternatives were considered including going to masked MOS ROMs which would consume much less

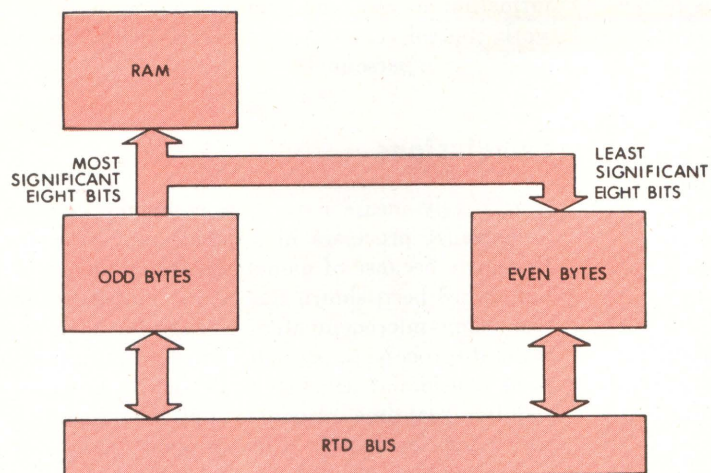


Fig 5 RAM as used in 16-bit mode of operation. Even addressed bytes are least significant eight bits while odd addressed bytes are most significant eight bits

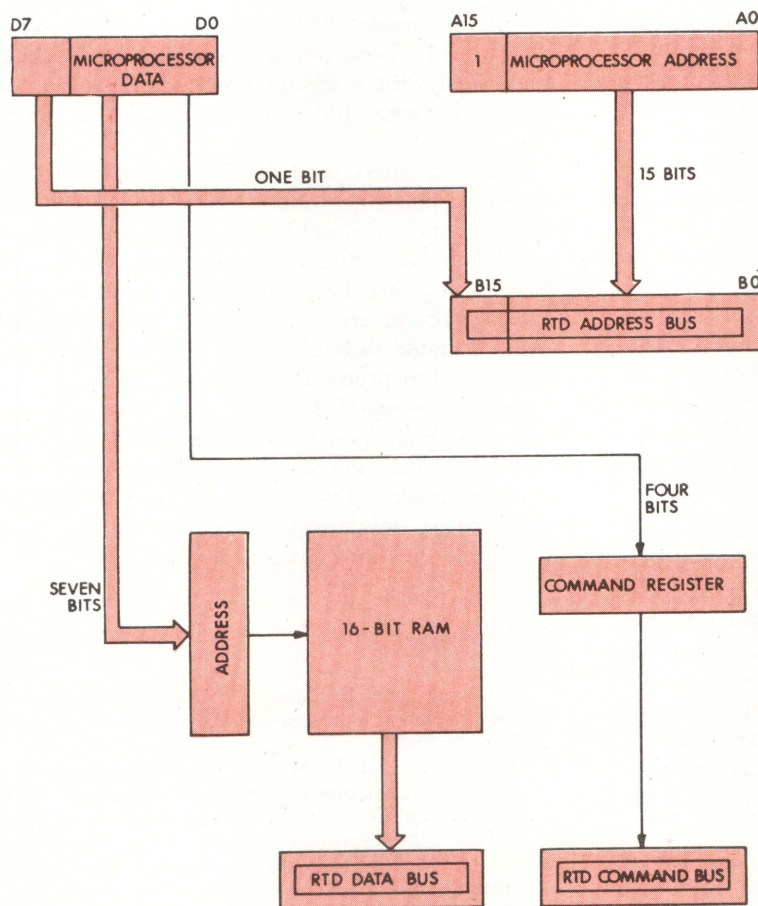


Fig 6 Bus master mode. Any write to memory with bit 15 of address set to one is interpreted as an RTD command. Least significant microprocessor address bits along with most significant data bit form 16-bit RTD address. 16 bits of data come from RAM as addressed by least significant microprocessor data bits. Command register has previously been loaded by microprocessor I/O instruction

power.³ The solution finally reached was to use power switching, that is, simply to switch on the 5-V supply only when the p/ROM is accessed. This power switching technique had no effect on the microprocessor operating speed but reduced current flow to p/ROM to only 0.11 A. The p/ROM power reduction of about 66 to 1 is highly significant in multiprocessor systems.

Offline Memory Mode

A ribbon cable connector is included on the front panel of the microcomputer module. This connector permits test personnel to plug in an external memory which logically replaces the "onboard" memory, a capability that has proven very valuable for program debugging

because it allows an access point for a ROM simulator.

Another important use of the access connector is offline testing of other modules installed in the data switches and multiplexers. Test personnel can utilize a program memory which contains comprehensive module diagnostics. In this offline mode, the microcomputer becomes a programmable module tester which can greatly aid in the isolation of malfunctions in a field environment, thereby facilitating fast and accurate module replacement.

Diagnostic Testing

Data switches and multiplexers are constantly undergoing three basic types of verification tests; the basic microcomputer as shown in Fig 4 is used for this testing.

Self Test—Self tests are done by the individual modules, with results stored in a status register which is read by the microcomputer.

Parameter Verification—Each module has certain parameters set up by the network manager as part of the network configuration. Items such as data rates and protocols of low speed channels and bandwidth allocation on the high speed trunks are transmitted from the network manager to the local microcomputer, which is responsible for loading these parameters into the working modules and verifying that they have remained intact. One of the design constraints placed upon module designers is that any parameter that is written to a module over the bus must be capable of being read back for verification. Since these parameters are stored in volatile memory on the various modules, it is very important that they be constantly monitored. In some cases, the local microcomputer can directly reload the module; in other cases, the network management system is asked to reload the module.

Signature Test—Each module within the data switches and multiplexer has an assigned identification code. The microcomputer continually scans all physical locations within a chassis and verifies that the correct type of module is installed. Furthermore, the mechanical switches on the module are sampled as part of the module signature. Thus, it is virtually impossible to have the wrong module type plugged in or even to have a wrong switch setting without creating an alarm condition, effectively eliminating human error common to a large complex communications system maintained by service personnel with varying skills.

If a fault condition is detected, a decision is made as to whether it should be considered a major or minor alarm. Fault data are sent back to the network control center and printed on the network manager console, as well as displayed locally on a diagnostic control panel. Alarm conditions may be disabled (useful if the local operator is in the process of replacing a failed module), or reprogramming requests may be entered for a given module after another module has been installed. In summary, the diagnostic process scans all modules for status of the self tests; verifies the programming of all programmable modules; verifies that the correct modules are installed and their switch settings are correct; makes decisions on

the significance of fault conditions, displaying this information locally and transmitting it back to the network control center; and interacts with directions from local service personnel.

Conclusions

A relatively inexpensive microcomputer may be used to decentralize processes in a data communications system. Primarily because of modularity, reliability, and throughput, it has been shown that a distributed processing system using microcomputers is superior to a totally centralized processing system. Two processes which have been considered are the small switching process which requires real-time responses and the diagnostic process which may operate in a background mode.

The system utilized to study these processes is the M3200 Pacuit network, whose bus architecture allows multiple processors to be utilized to mechanize tasks. The basic single 8080A processor architecture, while effective for background diagnostic tasks, had to be augmented with a second processor, powerful DMA, and large-scale integration SDLC circuits in the small switch case.

Microcomputers used in this way have led to systems in which those items best centralized (such as configuration data bases and overall network control) are centralized in large minicomputer-based switches, and processes which are best distributed (such as diagnostics, data switching, error control, and data concentration) are distributed throughout the network using microcomputers as the processing elements. This distributing of processes has enabled centralized nodes to be concerned only with high level tasks while the detailed tasks have been left to the microcomputer. The hierarchy of control in the network is from a network management center to switch-based minicomputers, then to microcomputers, and finally to hardwired processors.

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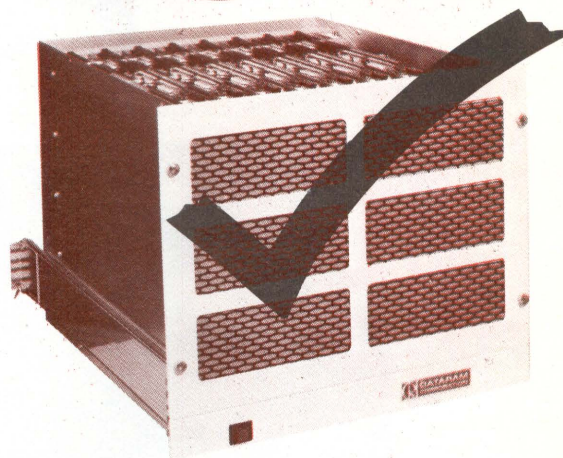
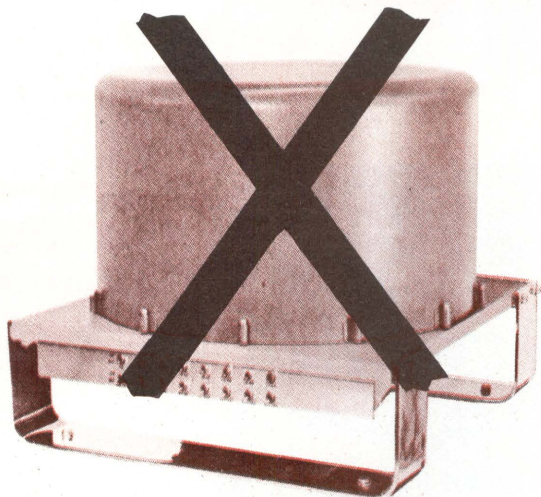
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Donald Mueller, a member of the technical staff of Computer Transmission, has had experience in detailed design implementation, product specification, and management of engineering resources. He received a BSEE degree from Iowa State University and has done graduate work at UCLA and Loyola.

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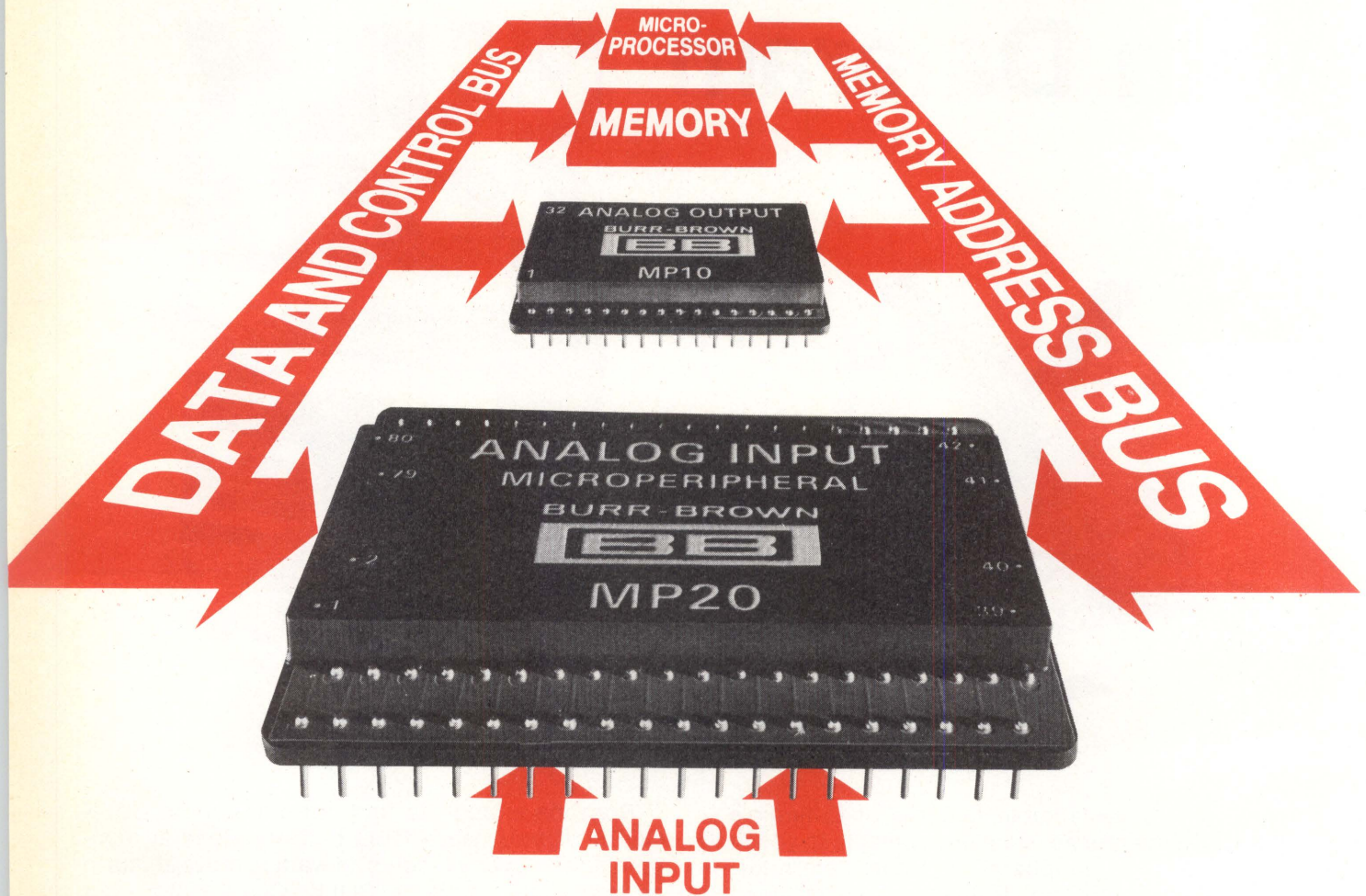
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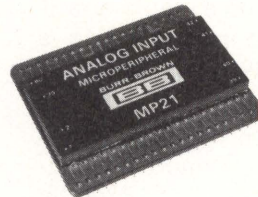
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Microcode Increases Minicomputer Processing Capability

Steven Buchwald

**Data General Corporation
Westboro, Massachusetts**

In software, high level languages and operating systems have contributed immensely to the availability of higher performance, more usable minicomputers; hardware breakthroughs have occurred in semiconductor memory and large-scale integrated circuitry. With each breakthrough, minicomputer technology advanced a quantum leap toward providing users with more powerful and wider application computation at lower cost. Now, another advancement, user-accessible microcode (microprogramming or firmware), is presenting system designers/microprogrammers with a more subtle, but highly effective processing tool. Properly implemented, custom-designed microcode enables users to get state-of-the-art hardware throughput rates from modern general-purpose minicomputers.

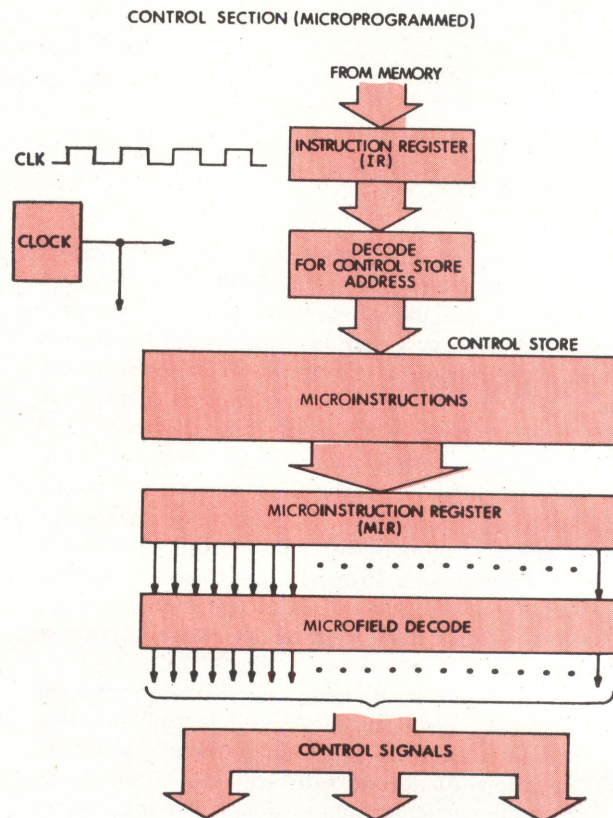
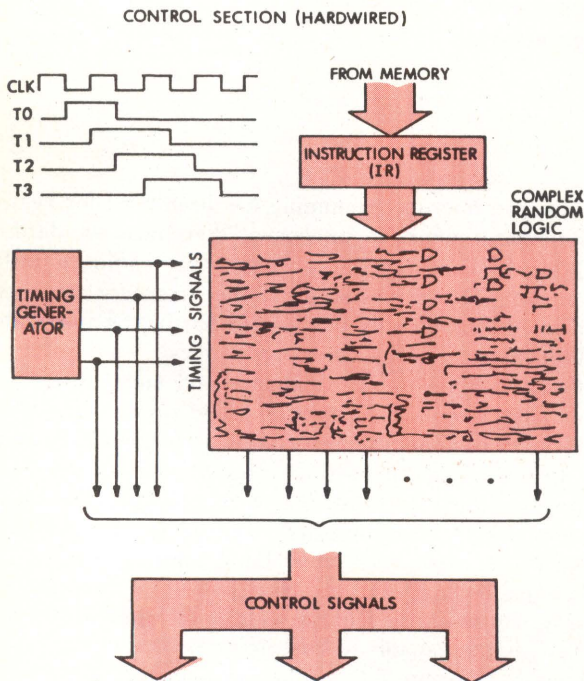
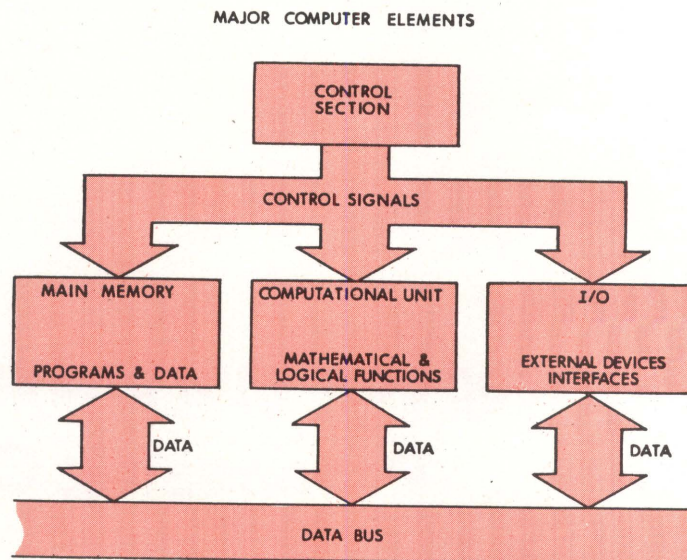
User-accessible microcode allows the microprogrammer to write extremely powerful customized instructions into the minicomputer's control processor to replace and combine the functions of normal software routines that may be critical to the particular application. Since the control processor executes at very high speed, and since several software routines can be combined into one firmware instruction, microprogrammed routines, once implemented and debugged, appear to the application as "extensions" of the minicomputer's own native hardware or micro-coded instruction set, rather than as slower executing software routines.

In fact, microprogramming has been used for years by computer vendors to implement their own standard and optional (floating-point or character-handling) instruction sets. This serves as proof that firmware can execute at speeds comparable to those of hardwired instructions. With user-accessible microcode, these vendors are, in effect, enabling users to enhance and augment the minicomputer standard instruction set to produce the equivalent of a custom-built, very high performance machine.

In order to achieve benefits of custom microcode, however, the user must deal with an expectable tradeoff—the degree of complexity required to fill each microword with the proper interrelated command, timing, and data path considerations. The power of microprogramming comes partly from a wide microword—perhaps 56 bits—that is capable of containing several parallel operations that execute during the same microcycle. However, just as assembly language is closer to actual processor logic than FORTRAN, microcode is closer still, and thus requires a solid understanding of all control processor functions and limitations.

A small amount of assembly code can greatly accelerate a program that is written mostly in FORTRAN, with the assembly code handling only the most critical routines, and the high level language doing more mundane chores. Many users will program 10% of the application—the critical real-time functions—in assembly language,

Fig 1 Hardwired vs microprogrammed computer control. In hardwired control section, machine executes by decoding contents of instruction register through complex system of random control logic which is synchronized by elaborate timing generator. In microprogrammed machine, instruction register contents are decoded to produce address of location in control store. Contents of that location are placed in microinstruction register (MIR) which can produce control signals directly, or through simple decoding of portions of MIR. A clock controls sequencing; each pulse brings a set of control signals into effect (Copyright 1977, Data General Corp)



and the other 90% in FORTRAN. Similarly, the key to effective custom-microcoding lies in identifying the most frequently used algorithms in the application program, and coding only those functions into microcode. By using microcode sparingly but effectively, the designer/microprogrammer can produce a 30 to 200% increase in overall minicomputer performance with just 1 or 2% of the program written in microcode.

Hardwired vs Microprogrammed Architectures

Currently, two methods of implementing instructions are being used: (1) designing machines with hardwired control logic, and (2) designing machines with microprogrammed control store. Fundamentally, the only difference lies in the control section design. The control section of a computer accesses three major functional elements—main memory, computational unit, and external input/output (I/O) devices—in both hardwired and microcoded implementations (Fig 1). In a hardwired machine this section is built from a complex system of discrete logic elements and sequential circuits which are often interrelated; in a microprogrammed machine it is built around an orderly array of microinstructions located in a special high speed memory called the control store. For both cases, each machine language instruction can be viewed as a series of elementary operations within the computer. In a microprogrammed machine, these operations are performed by executing microinstructions in the correct sequence. These microinstructions direct the activities of each data path, register, and processing portion of the computer, thus eliminating the need for complex hardwired control logic.

A hardwired machine (Fig 1) operates by fetching a machine language instruction from main memory and placing it in an instruction register (IR). The machine then executes this instruction by taking the contents of the IR and decoding them through a complex system of random control logic which is distributed throughout the central processing unit (CPU). Various elements comprising the control logic are synchronized by an elaborate timing generator which ensures that the operations required to execute the instruction occur in the correct sequence. Modifications to the instruction set generally require an extensive (and expensive) redesign of the fixed control section.

A microprogrammed machine (Fig 1) also operates by fetching a machine language instruction from main memory and placing it in an IR. However, the procedure for executing the instruction differs from that in a hardwired machine. Contents of the IR are decoded to produce an address which points to a location in the control store memory, whose contents are then placed in the microinstruction register (MIR). Control signals then can come either directly from the MIR or from a simple decoding of various portions of the MIR. Since each set of control signals required for any instruction can be held in the control store, a simple clock controls the sequencing needed. Each clock pulse brings the next microinstruction and, thus, the next set of control signals into effect. Modifications to the instruction set can be effected

simply by changing the contents of locations in the control store memory.

Application Analysis

Which applications can benefit from custom microcode? The primary criterion should be the fast execution of specialized instructions and frequently used algorithms. Most current applications are handled satisfactorily by general-purpose minicomputers with standard software. In an application where accelerated processing speed is important, however, custom microcode may make the difference, particularly in time-critical situations. If an application is performance-critical, it must contain a number of algorithms, or routines, that occur repetitively during the application program to qualify for a microcode prospect. An entire application is typically not coded into firmware unless it requires extraordinarily high throughput acceleration.

If the application is already programmed and running, repetitive routines can be easily identified for micro-

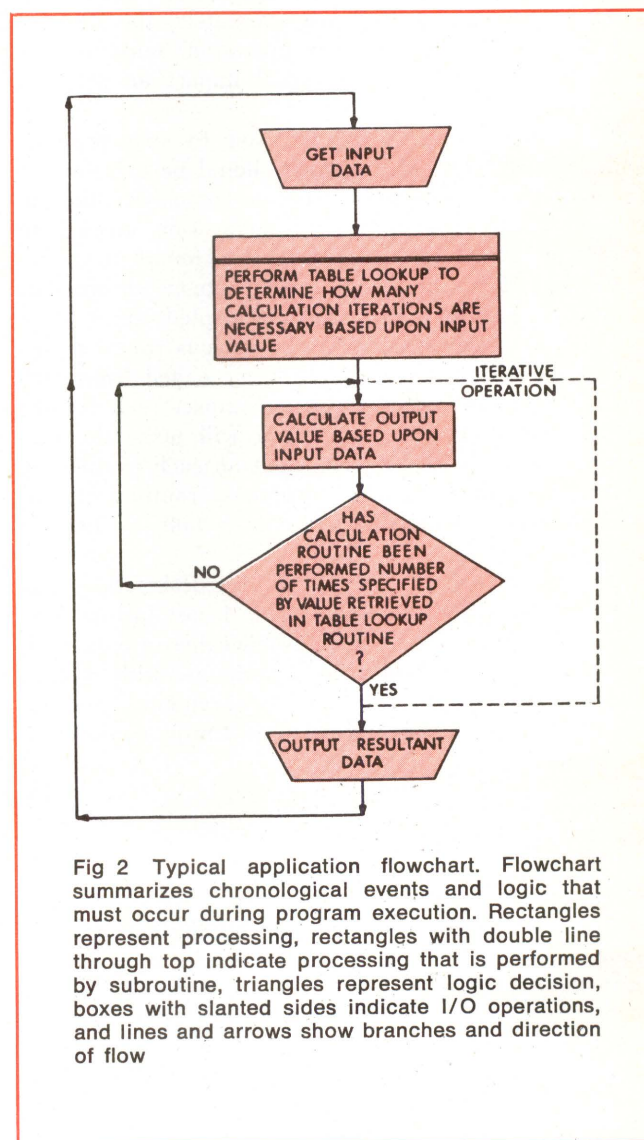


Fig 2 Typical application flowchart. Flowchart summarizes chronological events and logic that must occur during program execution. Rectangles represent processing, rectangles with double line through top indicate processing that is performed by subroutine, triangles represent logic decision, boxes with slanted sides indicate I/O operations, and lines and arrows show branches and direction of flow

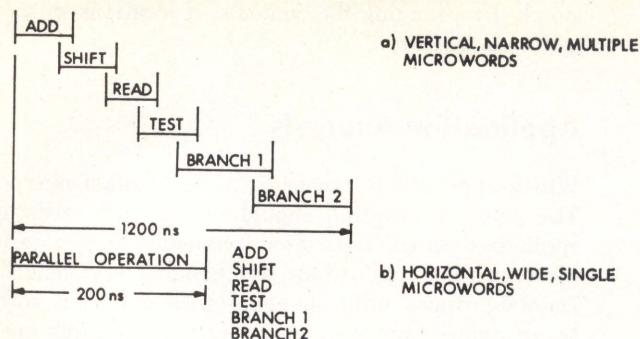


Fig 3 Horizontal vs vertical microcode execution. One wide word with parallel functionality does work of six narrow words, which have to operate sequentially to accomplish same arithmetic operation. Each horizontal word executes in one microcycle. Since cycle speed is function of control processor speed and not of word length, single wide microword performs operation six times faster than multiple narrow microwords

coding. If the application has never been programmed, it must first be broken down into its basic functional aspects, which will eventually become software subroutines. These might include, for example, I/O routines, table lookup routines, and calculate data routines.

Once organized into functional aspects, the application should next be represented by a flowchart, such as that in Fig 2, to reveal how these various functions interrelate. If the flowchart is constructed accurately, the iterative operations will be clear. These operations must then be evaluated in terms of their actual impact on program throughput.

As the application is analyzed, step by step, program bottlenecks that become apparent should be itemized for investigation. If, because of program complexity, the impact of iterative operations on application throughput cannot be accurately gauged, a benchmark program should be written in a high level language to simulate the application program. Once implemented, the application program can be run with the various routines, displaying the time entered and the time exited from each routine. This discloses the relative impact each routine has on overall program time, and will make the percentage of total program time spent on each routine apparent. Then, the most time-consuming routines can be set aside for microcoding in the actual application program.

The time and effort of highly skilled designers/microprogrammers will be dominant project cost factors. The microprogrammer should be knowledgeable in both computer hardware and software techniques, with a firm understanding of assembly level programming and familiarity with computer architectures, timing constraints, and data paths.

Microword Coding

The only thing "micro" about a computer microword is the level of detail needed to command the control processor to perform its basic functions in executing the microword. The word itself should be wide—32 bits or longer—so that certain commands can execute in parallel, within one microcycle, to produce powerful microcode. Too small a word limits parallel execution, and too large a word—more than 64 bits—can create undue programming complexity. A 56-bit, 15-field microword, shown

with field definitions in the panel "Microword Field Definitions" (opposite page), executes, in one microcycle, a number of "parallel" machine (control processor) commands, each from one to eight bits wide, that are contained in five major field groups. Parallel or horizontal implementation contrasts with a "sequential" or vertical approach, where a narrow microword requires more microcycles to perform a given algorithm.

As an example of the power of horizontal implementation, a single 56-bit, 200-ns microinstruction can read data to a control processor register from a previously addressed memory location while computing a new indexed address from any two general registers, containing 16-bit base and offset values. The microinstruction uses this effective address to issue a new memory start command, thereby incrementing a control processor count register to step the algorithm to the next calculation. It tests the result to determine whether the required number of steps has been reached, and thus determines the next microinstruction to be executed by selecting one of two full addresses within the current microword. In addition, the same microcycle may optionally test for pending program or data channel interrupts.

Microword Execution

The essential difference between narrow and wide word-lengths is in the degree of power and programming detail—wide words accomplish more operations faster, while narrow words are simpler to code and closer to assembly language techniques. A wide microword results in greater throughput—and fewer total words to code—than the more sequentially oriented narrow word.

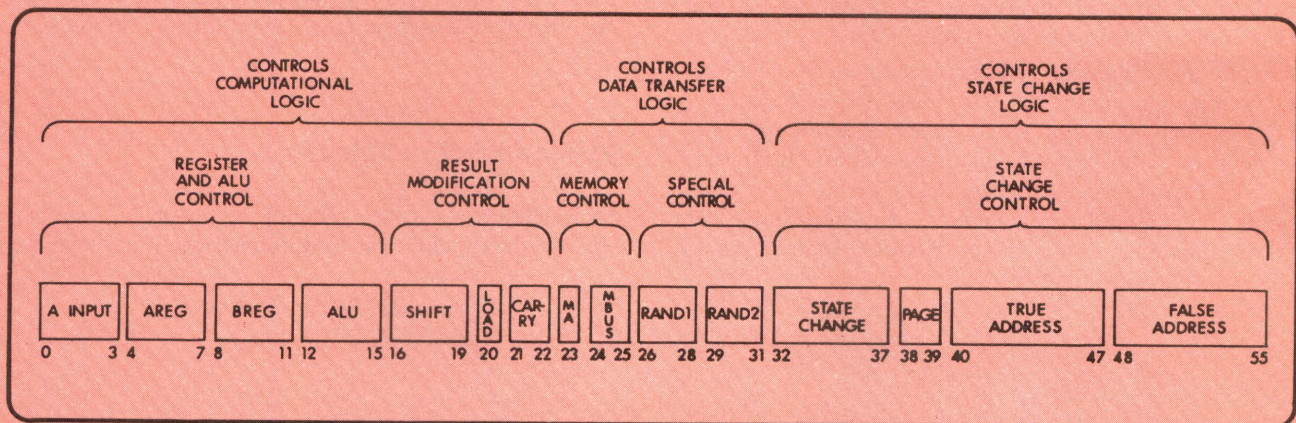
A computer with a narrow microword may require up to six microcycles to perform a basic arithmetic operation such as

- (1) Add two numbers
- (2) Shift the results
- (3) Read data from main memory
- (4) Test result of arithmetic operation
- (5) Branch to proper routine if test is met
- (6) Branch to proper routine if test is not met

As shown in Fig 3, this operation will take a wide microword just one microcycle, or one-sixth the time,

Microword Field Definitions

Field	Function	Field	Function
A INPUT 4 bits	Selects source of A bus, which is A input of ALU	MA 1 bit	Starts a memory module
AREG 4 bits	Selects one of eight registers in register file to be A register for current microinstruction. This register may be used as source of A bus and/or be loaded by shifter logic	MBUS 2 bits	Controls use of memory bus and current memory module
BREG 4 bits	Selects register from register file to be B register for current microinstruction. This register is used as B input to ALU and may be used for transfers to or from memory bus	RAND1 3 bits	Specifies one of six special control functions
ALU 4 bits	Selects one of 16 functions (nine arithmetic and seven logical) to be performed by ALU on its A and B inputs	RAND2 3 bits	Specifies one of seven special control functions different from those of RAND1 field
Shift 4 bits	Controls shifter logic and link bit to select one of 13 shift operations	State Change Test (6 bits)	Specifies the state change test to be performed
Load 1 bit	Determines if shifter logic output is to be loaded into A register	Page 2 bits	Supplies page bits for address of next microinstruction, or specifies source of true address bus
Carry 2 bits	Controls carry bit and enables special CPU logic for two accumulator multiple-operation instructions	True Address 8 bits	(1) Supplies low order eight bits of control store address when state change logic selects true address bus, (2) 8-bit constant to A bus, (3) address to scratchpad memory
		False Address 8 bits	(1) Supplies low order eight bits of a control store address when state change logic selects false address bus, (2) Allows stops to be suppressed by state change logic; and (3) Specifies address in current sector and page to which control is to be transferred when a state change test condition is false



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to execute. Narrow microwords do not execute faster—cycle speed is primarily a function of the control processor implementation technology. Is it worth the extra programming power to implement a wide microword? Although that depends on the critical nature of the application, it should be remembered that the algorithms, which are being microcoded, are the most critical operations in the program; if they need to be accelerated, they probably should be accelerated as much as possible.

Efficient coding of the microword, whether narrow or wide, requires “think-ahead” logic to any special timing

considerations among the commands to be used. Once these values are known, commands can be “plugged in” to their proper slots in the microword lineup so that they will execute with great efficiency.

This means, for example, that if data must be read from main memory at some point in the microprogram, memory-select timing must be taken into account when coding the microwords. If memory-select takes 200 ns and each microcycle is 200 ns, the memory module must be time-selected prior to the actual read command, as shown in Fig 4. I/O procedures and other operations with

unique timing constraints must be accounted for in the same manner.

Control Processor Requirements

Since the real power of a microcoded instruction set is derived from a combination of microword length and control processor, certain fundamental control processor capabilities must be examined when evaluating the performance potential of custom microcoded instructions. These include a powerful arithmetic/logic unit (ALU), a number of general-purpose registers fully dedicated to the microprogrammer, local data storage for intermediate results, and the range of parallel functions that can be performed in one microcycle.

Because of the fundamental nature of its operation, the ALU should be able to handle complex operations such as multiply and divide as readily as simpler arithmetic operations such as add and subtract. In addition, since programming logic is based upon performing a test and then jumping to one of two instructions (or routines) based on the results of the test, the control processor should permit conditional branching within each microword. Without conditional branching incorporated into each microcycle, three additional instructions may have to be coded: TEST, JUMP 1, and JUMP 2. With conditional branching within each microword, one microinstruction can be used to replace the three instructions, thus saving program execution time.

An important control processor component is a high speed scratchpad memory for rapid data access. Consisting of multiple fast storage registers, a scratchpad can provide storage space for temporary values, eliminating the need for accessing the minicomputer's slow main memory. Just as on a system level accessing data from a minicomputer's main memory is faster than going to

I/O bulk memory, so is accessing to a 200-ns scratchpad register more efficient than using the processor's main memory. Scratchpad capacity requirements will vary depending on the number of temporary variables and microroutine control parameters, but a comfortable scratchpad should offer between 64 and 256 locations to the microprogrammer.

Related to the application and overall microcode functionality is the memory medium to be used for actual microcode storage. Typically, the computer designer has two choices, random access memory (RAM) or programmable read-only memory (p/ROM). RAM is suited to applications where data or the microprogram will be changed or rewritten, since RAM can be erased. p/ROM, which cannot be erased or changed after initializing, is typically used for nonvolatile storage of permanent or proprietary microroutines, as in volume production or tight security applications. Users may write and debug microprograms in RAM, then simply transfer the fully debugged microcode into p/ROM for volume production equipment.

Another control processor capability that can be beneficial is parity-type error detection. Commonly used in semiconductor memories, a parity scheme adds one "check bit" to each word read into memory, setting up a consistent "even" or "odd" bit pattern. Later, the parity value is computed when the word is read from memory to ensure that parity has not changed due to a lost bit. Microcode parity adds a convenient check against the possibility of a control processor timing flaw by flagging any dropped bits that may occur during microprogram execution.

Minicomputer Selection

Minicomputer selection should be made by comparing microcode capabilities of different machines with appli-

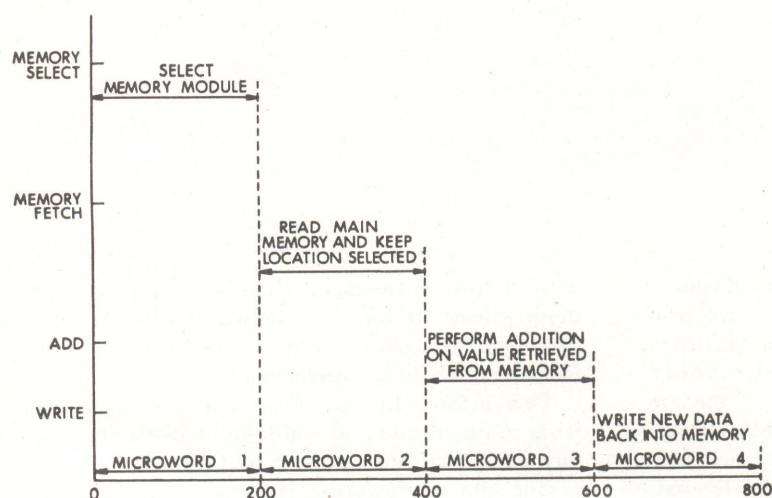


Fig 4 Timing considerations. Steps necessary to bring value from main memory into control store, modify value by performing arithmetic operation on it, and restore modified value to memory location. A second select command is not necessary for write command since read instruction kept that memory location selected. Memory select and read microwords (microwords 1, 2, and 4) are free to perform other operations when using wide microword. This means that no time is wasted performing these operations when they are executed prior to needing data

cation requirements. At the same time, however, the designer/microprogrammer should scrutinize the minicomputer's standard capabilities—instruction set, architecture, main memory range and type, processing throughput, I/O interrupt handling—just as carefully as the machine's microcode functionality. The minicomputer should be competitive in non-microcode as well as microcoding capabilities to operate a truly effective microcoded system. If custom microcode is used for what should be routine operations, such as I/O processing or certain floating-point operations, microprogramming time and effort will not be utilized efficiently. Custom microcode should be used only to accelerate application-specific bottlenecks; the machine's standard architecture should implement the remaining program.

To compare user-microcode capabilities, the designer/microprogrammer can examine how the computer vendor has used microcode in building standard and floating-point instructions. A minicomputer's microcoded floating-point instruction set allows ideal performance comparisons between different machines. Because floating-point operations are relatively complex, they require multiple microinstructions; and because all minicomputers perform essentially the same floating-point operations, direct comparisons can be made easily. Vendors make optimum use of microcoded instruction capabilities when building microcoded instruction sets.

System Integration

In a dedicated customized application, microcode can be easily implemented. However, if microcode is to be used within a larger multitasking or multiprogramming system, extra caution must be exercised to prevent microcode activity from impeding other system functions.

Users in a timesharing or multiprogramming environment should not load the writable control store with their own microprogram, due to its preemptive nature. Once the minicomputer's operating system yields to the microprogram, that microprogram may override scheduling and priorities of all other system functions, and not allow interruptions by the operating system to let a random user demand be processed. In addition, if a microprogram that is not fully debugged runs in a timesharing or multiprogramming environment and crashes, it can crash all other users as well.

In a multitasking system, where all possible use demands are known, the operating system can be scheduled to assign control to the microprogram at a time when no other task will want to interrupt. Therefore, the microprogram should not take longer to execute than the most critical response times of other system tasks. For example, in a multitasking system where five devices require servicing every 50 μ s and two of the devices have a 20- μ s response time, the user-microprogram must at worst case execute in fewer than 20 μ s.

In such a system, it can be beneficial if the minicomputer's microcode unit contains a direct memory access (DMA) interrupt feature. DMA allows large blocks of data to be transferred at high speeds from I/O devices into the computer in a single interrupt, whereas programmed I/O requires an interrupt for each word transferred. A sophisticated microcode control processor will permit DMA transfers during microprogram execution.

Control Processor Example

The Eclipse® S/130 control processor (Fig 5) is driven by a 56-bit microword with 15 independent control fields. By achieving a high degree of functional parallelism in each 200-ns microcycle, this processor retains the flexibility and economy of microprogramming while approaching the speed of hardwired logic. In each microcycle, internal parity hardware provides a self check of the timing margins through the control processor's storage, logic, and bus elements. Control store memory contains 1024 words using RAM, or 2048 words using p/ROM, for holding (storing) user microprograms and data.

State change logic determines the next microinstruction to be loaded into the 56-bit 15-field microinstruction storage register by selecting a 12-bit control store address from one of two sources—the true address field or the false address field. The false address field specifies an exact address while the true address field may be modified by either the micro-address register (MAR) and/or the instruction register (IR). Microinstruction decode logic decodes the contents of each field to produce the control signals that operate the CPU.

CPU computational logic is built around a register file, an arithmetic/logic unit (ALU), and a shifter. Basic data flow is from the register file to the ALU, from the ALU to the shifter, and from the shifter back to the register file.

The register file contains eight 16-bit registers. These registers are gated across A and B register buses to the ALU. Four of the registers are machine language accumulators, another is a program counter, and the remaining three are general-purpose registers. These registers are available only to the microprogrammer and can serve as temporary storage devices. Every microinstruction selects an A register and a B register from the register file; the same register may be selected as both A and B register. The contents of the selected registers appear as the respective A and B outputs of the register file. The A output, or part of it, may be selected as a source for the A bus; the B output is the B input to the ALU. A microinstruction may specify that the A register be loaded with the output of the shifter at the end of the current microinstruction. It may also specify that the B register be used as a source of destination for memory (MEM) bus transfers.

Supplying the A input to the ALU, the A bus has 12 sources, any one of which may be selected by a microinstruction. These sources include zero loading, one of two microcoded constants taken from the true address field of the instruction currently in the 56-bit microinstruction storage register, one of three forms of the IR, a bit mask from the bit decode logic, a 16-bit word from the program load ROM, and the contents of the A register in one of four forms.

The ALU has two 16-bit inputs called the A and B inputs, and one 16-bit ALU output. The A input is from the A bus and the B input is from the B register. Any one of nine arithmetic or seven logical functions may be performed by the ALU on its inputs, as selected via the ALU field of the current microinstruction. Output from the ALU can be gated onto the MEM bus, the logical address (LA) bus, and the shifter.

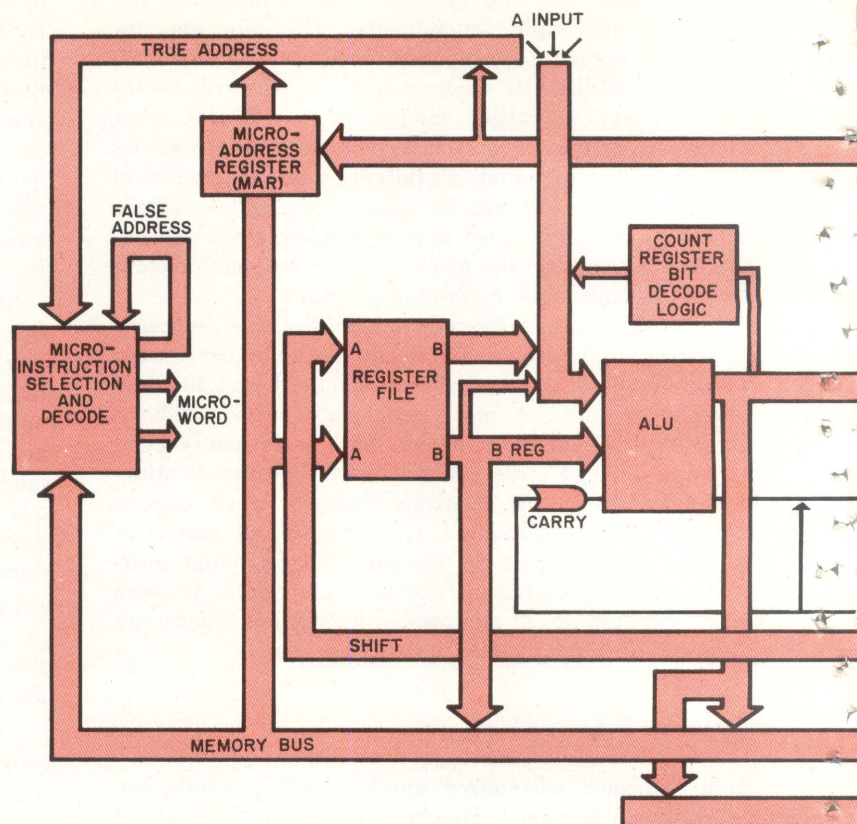


Fig 5 Control processor functional elements. Microprogrammers must familiarize themselves with data transfer buses, register paths, and functional elements of control processor before attempting to write microcode. Computational section includes register file, ALU, and shifter. Register file is gated across two buses to ALU; 16-bit output from ALU goes to shifter, which performs one of 13 operations. Shifter output is gated back to register file, completing flow. Scratchpad data move along memory bus to ALU result, register file, or to main memory

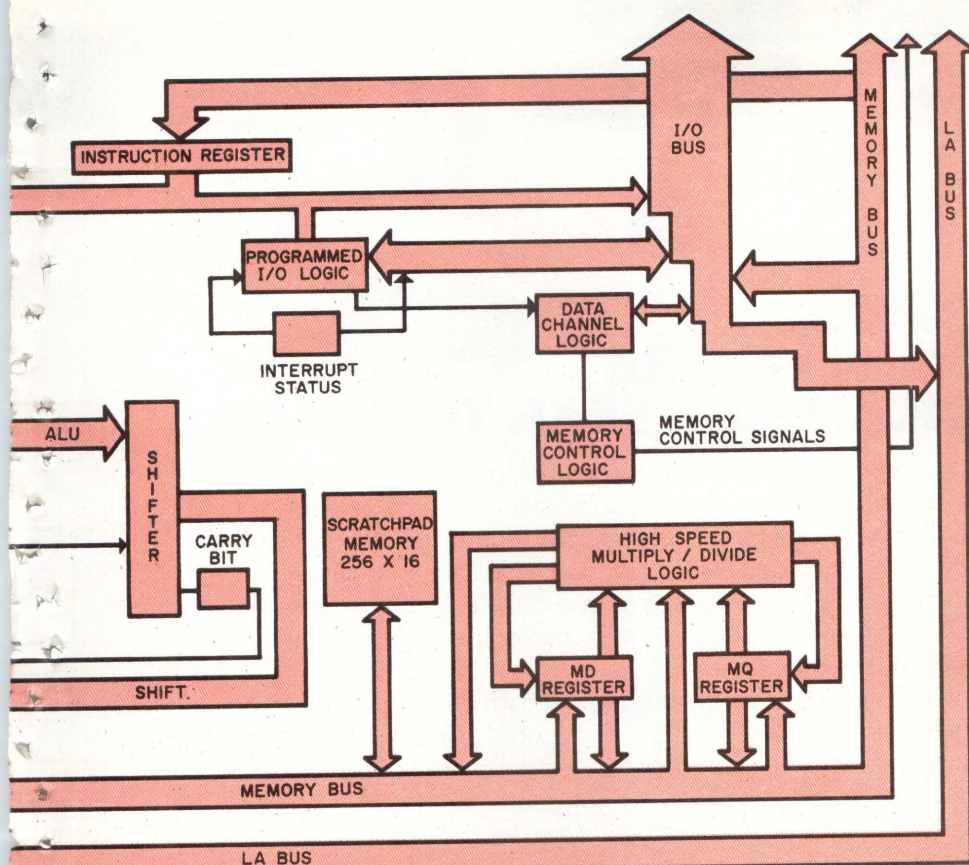
After it has modified the output of the ALU, the shifter places the modified result at the A input of the register file. The shifter may shift its input left or right one bit, may interchange two 8-bit bytes, or may perform any one of 13 operations, as directed by the shift field of the current microinstruction.

Scratchpad memory offers the microprogrammer the added fast access storage useful in complex microroutines, and consists of 256 16-bit registers. Scratchpad is addressed by the eight least significant bits of the true address bus. Data in the scratchpad are transferred along the memory (MEM 0-15) bus and may be gated into the ALU result, the register file, or main memory. Direct data transfers are possible between the floating-point (multiply/divide logic) unit and the scratchpad.

Two additional 16-bit registers (MD and MQ) can perform as a 32-bit shift register. The multiply/divide logic includes an adder and a shifter that run in 100 ns and may be cycled twice within one 200-ns microcycle. Data may be loaded into the MD and MQ registers from the memory bus or the scratchpad memory and trans-

ferred out in the memory bus or directly into the multiply/divide logic.

The microprogrammer can easily transfer data to and from main memory. To accomplish this, the logical main memory address is transferred from the ALU to the LA bus. Data are transferred between the CPU and main memory across the memory bus. Memory operations are divided into two steps called half-cycles. When a memory module is selected (started), the first or access half-cycle is initiated. During this half-cycle, data are read from memory into a buffer in the memory module. When the module is released, the second or restore half-cycle is initiated. During this half-cycle, data are written from the buffer into memory. In order to start a memory module, the CPU places an address on the LA bus and issues a start signal to main memory. To complete a read operation, a second command is given which transfers data from the memory buffer onto the memory bus. On a write command, data are transferred from the memory bus to the memory buffer. In either case, the buffer contents eventually get written back into memory.



Summary

Like earlier computer technology breakthroughs, user-accessible microprogramming holds the promise of greatly increased minicomputer performance at relatively low cost for the system designer/microprogrammer who fully understands the application needs and the workings of microcode. One difference is that microprogramming is not a "bolt-on" enhancement. Its effectiveness is a function of the user's knowledge of the application first and the microprogramming technique second.

The performance-conscious designer/microprogrammer should first evaluate the appropriateness of customized instructions for a particular application, and then investigate and learn about microprogramming as thoroughly as possible. Once fully understood, the benefits of microcode will emerge, and the designer will be able to harness this powerful technique to produce state-of-the-art performance with general-purpose minicomputers. These benefits include accelerated processing speed, fast execution of specialized instructions and most-used al-

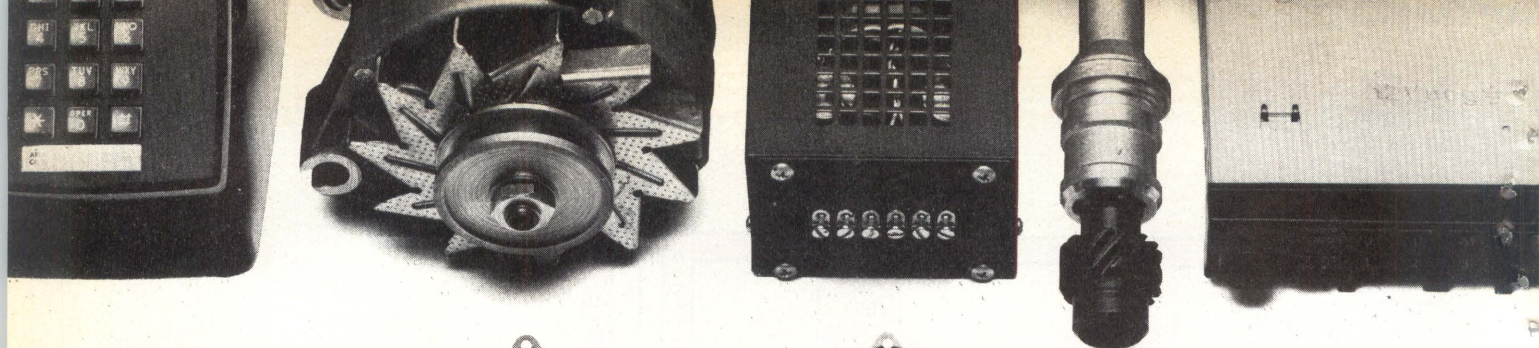
gorithms, and generation and debugging of extensions to the computer's own instruction set.

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Flat panel matrix displays have been improved to the point that they can now be considered for many applications that were formerly the exclusive domain of the CRT

Flat Panel Displays Offer Graphics Alternatives

Joseph W. Aichroth

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Accepted by many as a permanent fixture, the venerable cathode-ray tube (CRT) has been the standard display in electronic applications for more than 40 years. While its drawbacks are well known (size, weight, fragility, and high voltage), CRT popularity has never been higher—it is a good visual interface at moderate cost by a well-established manufacturing process.

However, competition is evolving. Several types of flat panel displays are challenging the CRT in certain applications. At this time, a simple display replacement for the TV picture tube is not available, but computer graphics displays—such as instrument panels on aircraft or automobiles—soon will incorporate the rapidly emerging flat panel technology.

In rudimentary form, some types are already in everyday use. A digital watch or pocket calculator uses a liquid-crystal display (LCD) or a light-emitting diode (LED). Older digital instruments (before LEDs) usually used a plasma (gas-discharge) display. These three major display technologies—LCD, LED, and plasma—have been undergoing significant improvements. No longer do they simply read out numerics or alphanumerics. They are presently being built in dot matrix formats, with the flexibility and resolution to display virtually any symbol or graphic.

Still other electro-optical technologies are available. Incandescent bulbs are ideal for outdoor signs and athletic scoreboards, but they have very limited applications elsewhere; and although electroluminescent panels periodically receive publicity, their early promise has

never been fully realized. In addition, some laboratory experiments have used either suspended magnetic particles or magnetic bubbles as displays, but these devices have not successfully made the transition from laboratory to production line. Therefore, this discussion will cover the state-of-the-art, capabilities, and applications of the LCD, LED, and plasma matrices—the three major flat panel display challengers to the CRT.

Liquid Crystal Display

Although the designation seems contradictory, liquid crystal material exhibits certain electro-optical properties when its state is maintained between liquid and crystalline. If the material is very cold (typically below -10°C), it crystallizes. As liquid crystal becomes warmer, the display gets weaker. At about 60°C , the material loses its electro-optical properties entirely.

Fig 1 shows a simplified cross-section of liquid crystal material encased in a "sandwich" of two glass plates. Each plate has a conductive coating on the inside surface, and the coatings are etched (in mirror images) to form appropriate graphic symbols. When a voltage is applied across the liquid crystal material, its optical characteristics are altered and the symbols become visible.

Liquid crystal itself does not generate light; it depends upon external source stimulation. If the glass plate behind the display is transparent, readability depends upon light passing through from the back. Alternatively,

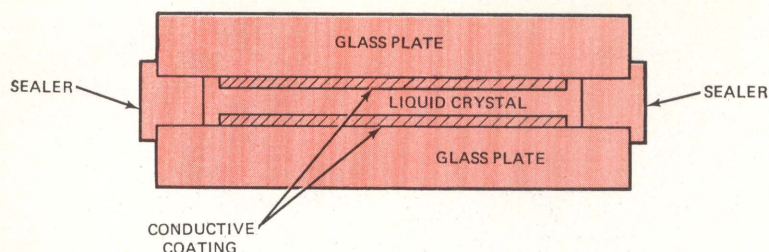


Fig 1 Cross-section of LCD. Optical characteristics of liquid crystal material change when potential is applied. Characters or dots are shaped by masking

if the back plate has a mirror finish, the display depends on reflected light from the front.

This dependence on external light is both an advantage and a disadvantage. The stronger the ambient light, the easier it is to read liquid crystal symbols. However, the symbols can not be read in the dark without an external light source.

Light-Emitting Diode Matrix

This matrix uses LEDs mounted on a glass or alumina substrate, as shown in Fig 2. Since each LED is its own light source, each may be addressed individually through an X-Y or rho-theta (circular) matrix. Any desired number of LEDs may be lighted simultaneously.

While the idea of an LED matrix is not new, early attempts were limited by the state-of-the-art. The LEDs themselves were too big, and the spacing necessary for manufacturing too great to allow adequate resolution for many purposes. Now, however, miniature LEDs have been combined with thick film hybrid manufacturing processes to achieve resolutions up to 50 LEDs/in (19/cm).

Plasma Matrix Display

The plasma matrix display (PMD) is enclosed by two glass substrates, each of which carries a set of parallel electrodes. Two sets of electrodes run at right angles to each other to form an X-Y matrix. Some PMDs use a center plate with a hole at each X-Y intersection. A gas-

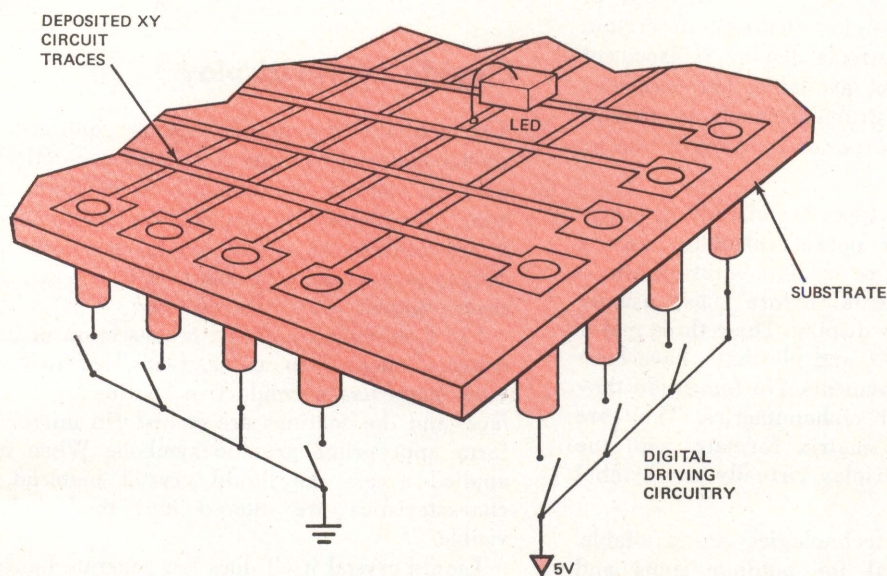


Fig 2 Typical LED matrix. LED matrix is thick film hybrid composed of individual LEDs on alumina substrate. Row-column addressing offers complete flexibility

discharge cell placed in each hole lights when a voltage is developed between the two electrodes.

A further refinement eliminates the gas-discharge cells, as shown in Fig 3. A transparent dielectric coating is applied on the inside of the glass substrates. Electrodes are embedded between the substrate and the coating. With gas (typically neon) between the two coatings, discrete charges can be stored on the film surface. Thus, a gas discharge occurs at the intersection of the two charged electrodes, just as in the gas-cell method.

Size and Weight

Although they share the same general matrix format, the properties of the three major flat panel display types differ markedly. Therefore, they must be properly evaluated in light of the specific requirements of each potential application. For some applications, such as aircraft instrument panels and portable equipment, size and weight are critical parameters. Here, all three matrix displays have dramatic advantages over the CRT. The three display types are basically flat [less than 0.5" (1.27 cm)], although there is some thickness variation between the types. Because it uses only a single substrate rather than a glass envelope, the LED matrix is somewhat thinner and lighter than the others, typically less than 0.125" (0.318 cm) thick and about 0.5 oz/in² (2.2 g/cm²) or about half the weight of the other two types.

Resolution

For sheer high resolution, the CRT has the advantage. Since the three matrix displays all rely on physically discrete elements, they are limited to achievable manu-

facturing tolerances—currently about 40 to 60 lines/in (15 to 24/cm). For comparison purposes, this is roughly equivalent to the resolution on a television CRT with a 10" (25 cm) vertical dimension (using the 525-line raster standard of the United States). Of course, matrix displays do not suffer from such CRT ailments as focusing problems or burns in the screen caused by high intensity.

Visibility

Ability to read the display varies substantially with ambient light. For liquid crystal, the brighter the environment, the easier it is to read. By contrast, plasma displays, LEDs, and CRTs are all light generators; they become more visible in a darker environment.

The LED matrix produces a brighter display as increasing current is supplied to the LEDs. A photocell can be used to regulate current according to ambient light. Experiments have shown that an LED display can still be read satisfactorily when fully illuminated by a high intensity photoflood lamp placed 3 ft (0.9 m) away.

On the other hand, the plasma matrix is a threshold device. Its gas-discharge cells either fire or they do not. Intensity variation is achieved through current limiting or duty-cycle control. Examination shows that plasma matrix visibility is typically comparable with that of an LED matrix when the LEDs are driven at about the mid-range of the intensity scale. Neither display suffers as much washout as the CRT at high ambient light levels.

Reliability

Although liquid crystals were plagued by early reliability problems, these have been largely overcome. Current

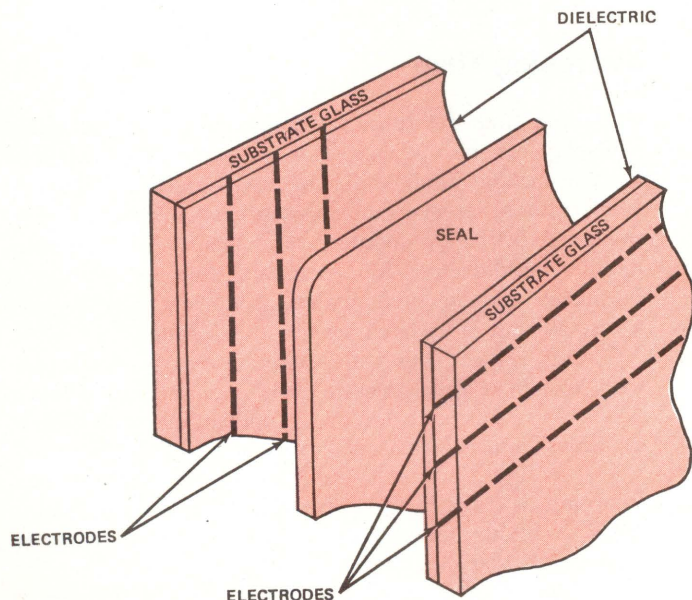


Fig 3 Plasma matrix structure. Gas in plasma matrix display is enclosed in glass "sandwich." Electrodes screened on glass permit row-column addressing

information indicates that the expected life of liquid crystal now approaches that of the plasma matrix—in some cases as high as 50,000 hours. This is somewhat better than a CRT, although substantially less than the 100,000 hours normally expected from LEDs. Of course, any matrix display also has the advantage that a failure is rarely catastrophic, with the possible exception of a gas-seal failure in the plasma matrix. Failure of a single element in a matrix is not likely to seriously diminish the display's readability.

Color

To the eye, color is composed of both hue and saturation, with the saturation often referred to as the gray scale. Hues are not presently available in liquid crystal where the choice is between light points on a dark background or dark points on a light background. However, development in fluorescent-activated LCD should offer color in the red-green region in the near future. While some work has been done on providing a gray scale, the possibilities appear limited for liquid crystal.

The plasma matrix typically uses a neon gas to produce an orange glow. Some variation in color can be achieved by using a gas mixture or additives. Another method is to use different gases in the cells at different x-y addresses. Because of its threshold nature, the plasma matrix provides no gray scale.

Color choice in the LED matrix is limited by the LED colors available. Present choices include red, green, yellow, and infrared. Manufacturers have been working to produce blue, but have yet to be successful. Unlike the plasma display, the LED matrix is not limited to a single color. One version of the LEDSCREEN,* which is made up of red and green LEDs mounted in pairs, provides true 3-color capability (Fig 4). A red and green pair are lighted together to produce yellow. Since the light produced by an LED is proportional to the current flowing through it, the matrix is capable of a nearly unlimited gray scale.

Power Requirements

When low power is the deciding application factor, liquid crystal is the unquestionable choice, as long as no auxiliary light source is required to read it in the dark. Low power is the main reason liquid crystals are so attractive to digital watch manufacturers. Typical current drain is substantially less than $1 \mu\text{A}/\text{cm}^2$. Since drive voltage is typically in the 3 to 6 Vac range, liquid crystal is directly compatible with all standard types of solid-state logic circuitry. However, ac drive voltage is required, since any dc component would drastically shorten the display life.

Power drawn by any matrix display, of course, depends on how many points are lighted. Both plasma and LED matrices lend themselves to multiplexing; thus, individual points are operated at a reduced duty cycle. This not only saves power, it also enhances visibility. For example, an LED which receives a peak current of 40 mA at a 25% duty cycle (50 to 60 pulses/s) will normally appear slightly brighter than if it received a continuous 10 mA.

While current drain is similar for plasma and LED displays, voltage requirements are much different. LEDs

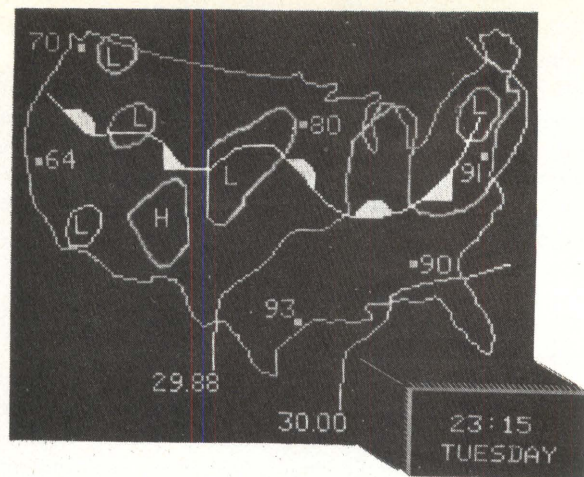


Fig 4 LED matrix for graphics. LED matrix, using red and green LEDs to obtain yellow, can be expanded to any desired size using stackable modules. Resolution up to 50 LEDs/in can be achieved using miniature LEDs combined with a thick film hybrid manufacturing process (Photo courtesy of Integrated Microsystems Inc)

operate from normal 5-Vdc logic levels, while a plasma display requires a power supply delivering 125 to 160 Vdc to initiate the gas discharge. This, of course, gives LEDs a distinct advantage wherever low operating voltage is important, such as an aircraft or a portable application. This advantage over high voltage systems, such as the CRT, is even more pronounced in critical environmental applications—in hospitals and laboratories, for example. Operation at logic levels also simplifies the designer's task in interfacing with transistor-transistor logic (TTL), complementary metal-oxide semiconductor (CMOS), and other logic circuitry.

Switching Time

Switching time determines the maximum rate at which a display can be updated. The necessary rate is defined by the specific application. In some cases, a relatively small rate difference can substantially improve performance. A 5 times/s update rate is adequate for an automobile speedometer, for example; however, setting a frequency counter to a critical frequency may require a display that is updated several times faster.

In this respect, the LED matrix is clearly the leader, with switching times measured in nanoseconds. Plasma displays are adequate for most applications, with switching times from $1 \mu\text{s}$ to 1 ms.

Just as liquid crystal is the clear winner in power consumption, it trails in switching time. While its operating speed is highly temperature dependent (it slows down as it gets colder), typical switching time is on the order of 200 ms. At that speed, the display can be updated at a maximum rate of 5 times/s.

*Trademark of Integrated Microsystems, Mountain View, Calif.

Environmental Considerations

Flat panel displays all perform well in a relatively stationary, room temperature, sea level environment. In hostile environments, however, operational differences are revealed. For example, the readability of liquid crystal at high light levels makes it attractive for aircraft applications where slow switching speed is no problem. However, operating temperature and altitude ranges are restricted for liquid crystal. Below about -10°C , it freezes, and above 60°C , it liquifies and becomes unreadable. In addition, liquid crystal operation is substantially degraded long before it reaches these extremes. At some increase in cost and complexity, the low temperature limit can be extended by incorporating heaters into the display. It is also intolerant of high altitudes. Unprotected, liquid crystal will burst at pressures corresponding to about 8000 to 10,000 ft (2.4 to 3.1 km). Enclosed in a pressure vessel, liquid crystal has been tested to 30,000 ft (9.1 km), but at the expense of some degradation in performance and safety.

Both plasma and LED displays operate over somewhat similar temperature ranges (typically 0 to 70°C). Their performance does not deteriorate substantially toward the extremes, and they are not particularly altitude (pressure) sensitive.

Since the LED matrix is totally solid-state, it can operate in a vacuum, and will tolerate more abuse than the glass envelopes of the plasma or liquid crystal displays. Operation of the plasma display depends on the integrity of the gas seal: as long as the gas does not leak, the display is unaffected by altitude. Development effort is continuing in both technologies toward meeting military-type environments. All three matrix displays withstand shock and vibration better than a CRT.

Radio-Frequency Interference

While any switching generates some radio-frequency interference (RFI), liquid crystal and LED matrices produce no more than any other equipment that uses standard digital logic level. However, the plasma matrix has the inherent noisiness of any gas discharge device. While this is not a problem for many applications, in critical areas the plasma requires careful shielding, as does a CRT.

Driving Electronics

Electronics required to drive a flat panel display are just as important as the display itself in terms of size, cost, and other parameters. Obviously, a CRT, for example, requires not only a high voltage supply, but also a great deal of associated deflection and drive circuitry. An additional disadvantage of the CRT in many applications is that it is basically an analog device. Thus, to receive digital signals, conversion circuitry is required.

All three types of matrix displays can be addressed directly in digital form. The "brute-force" method is to provide an electrode for each row and column, and drive each separately. However, significant savings in size, cost, and complexity can be achieved by scanning the displays by rows or columns. In this case, individual

points in the matrix operate in a pulsed mode, requiring that the entire display be scanned often enough so the eye does not perceive a flicker.

The primary factor in addressing is the switching time of individual elements; the faster the switching time, the larger the display. Thus, the best candidate for large displays is the LED matrix, with its very fast switching time. One design, composed of edge-stackable LED display modules, is more than 3 ft (0.9 m) square and includes more than 800,000 display points. Fig 4 shows an LED matrix used as a weather chart.

Plasma matrices are also amenable to multiplexing, although a large display requires a more complex scanning arrangement because of slower switching speed. Plasma displays of up to 8 in² (51.6 cm²) have been built, and larger ones have been proposed.

The liquid crystal display, with its slow switching time, is difficult to multiplex. This severely limits practical matrix sizes to perhaps 4 in² (25.8 cm²). Because of this limitation, liquid crystals are more amenable to a character-mask display (Fig 5) than to a dot-matrix format.

Cost

Since all three matrix displays are what might be called "emerging technologies," cost projections are perhaps the shakiest comparison of all. The most meaningful method is to compare them to the CRT, which is a mature technology. Installed cost of a high quality, instrument-size, monochrome CRT is typically in the range of \$20 to \$30/in² (\$3 to \$5/cm²). While any of the three matrix displays now runs several times that, none is yet in volume production. Best industry projections indicate that all will be cost-competitive with the CRT within two or three years.

Applications

Possible applications for flat panel displays can be generally divided into three broad classifications: stationary, portable, and vehicular. In a stationary application, such as a computer terminal, size, weight, power, and fragility are typically less important than, say, cost. Therefore, the CRT is likely to dominate this market for the next several years. However, matrix displays may soon begin to make some inroads (Fig 6).

Because of limited battery capacity, portable applications are particularly sensitive to power requirements. This, coupled with excellent readability in bright light, gives liquid crystal a considerable advantage—if its limitations do not interfere with the specific application. For example, the low power advantage is lost if external light must be supplied for night viewing. Also, slow LCD switching time makes it unattractive for such applications as portable measuring instruments. Both LED and plasma displays are more attractive than the CRT for most portable applications. Between these two, the plasma display has the disadvantage of requiring high voltage, which complicates power supply design.

Thus, the LED matrix appears to have an edge for most portable applications where the limitations of the liquid crystal can not be overcome. Furthermore, LED technol-

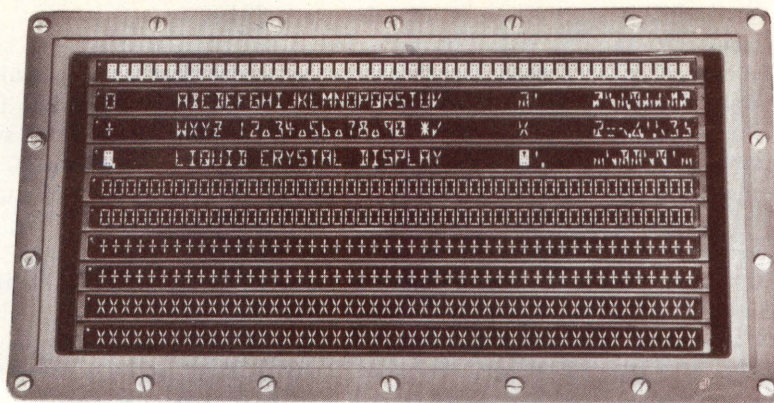


Fig 5 Character mask display. While liquid crystal displays to date have proven uneconomical in dot matrix form, they are attractive for alphanumerics. This one is intended for military applications (Photo courtesy of Applied Technology)



Fig 6 Plasma matrix display. Plasma display uses 5 x 7 dot matrix for alphanumerics. Similar arrangements can also be used for graphics (Photo courtesy of Burroughs Corp)

ogy is already being merged with fiber optics and sensors in production equipment.

Vehicles, cars, or airplanes are harsh environments for a display. In these, power is less important than ruggedness, readability, resolution, and reliability. However, size and weight are often critical requirements. Thus, much investigative effort is being directed at all three types of matrix displays. None has the inside track, although the LED matrix has some advantages because of its higher resistance to shock and vibration, its higher reliability, and its slightly smaller size.

Conclusions

It is apparent that the world of displays is changing, and that the changes will become increasingly evident during the next several years. While it is premature to predict the early demise of the CRT, it almost certainly will be replaced in more and more applications. Environmental considerations, size, weight, and power requirements all favor flat panel displays. While the CRT is still the leader in cost and resolution, flat panel displays are improving in both areas. No particular technology of the three major flat panel displays is likely to become

the all-purpose CRT replacement. Rather, all three are likely to be used extensively.


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Digital Controller for Microfiche Display Selection

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Medical College of Georgia
Augusta, Georgia

Any one of up to 1800 stored microfiche images is automatically selected by a UART-based digital controller for display by a servodriven viewer, enhancing computer-assisted education

The utility of computer-assisted instruction (CAI) would be greatly extended in certain educational areas if a large amount of stored photographic material could be readily selected and presented on a mechanical viewer as part of a predefined CAI program. Machine display of microfiche images under electronic circuit direction is an obvious choice.

This digital controller, described on a block diagram level, is capable of automatically selecting any one of up to 1800 stored microfiche images for presentation by a servodriven display machine. Controller circuits and associated microfiche display mechanism are designed to function as an integral system, adjunct to a remote computer terminal. The system control signal, embedded in the standard 8-bit ASCII-coded serial data stream from a modem to the terminal, consists of a nonprinting "alert" character; this character initiates storage of a specific number of fol-

lowing characters into the controller for microfiche image selection.

Currently used for computer-assisted medical education, the microfiche control system has considerable potential for application in other areas. Uses of the design principle for hardware control are suggested.

Display Machine Principles

The Bruning model 95 image retrieval machine was chosen for this application because it is an automatic, keyboard-operated machine with a storage magazine holding 30 microfiche carriers. The COSATI (Commission on Scientific and Technical Information) standard microfiche format with a 24:1 reduction ratio was chosen for optimum photographic resolution. Each fiche of this format contains five rows of 12 images each, with total storage in one magazine of 1800 images.

Microfiche carrier, image row, and image column selections in this ma-

chine are accomplished by means of two potentiometric servosystems. Analog voltage inputs to the systems are derived from passive voltage dividers operated by the pushbutton keyboard. Each microfiche carrier has a tab at a unique location extending from the back of the magazine. In a timed sequence, the microfiche carrier select voltage is first applied to the horizontal drive servo, which positions a "kicker" at the tab of the selected microfiche carrier. The tab is then struck by the kicker, and the selected microfiche carrier is driven into the display mechanism. Finally, the microfiche image row and column selection voltages are applied to the servomechanisms that project the chosen image onto the viewer. The image selection time sequence takes 4 s if the selected image is on a different microfiche carrier, but less than 1 s if it is on the same microfiche carrier (already in the display, or kicked, position).

Controller Requirements

Primary design requirement of the digital controller was that no separate interface could be implemented, meaning that microfiche selection control signals had to be in the ASCII 8-bit serial data stream transmitted by the modem to the remote computer terminal. Other considerations were that the user of the microfiche system would not be aware of the process of image selection and, since other noncomputer driven instructional material is available in microfiche form, that the machine could still be used in manual control mode.

A problem encountered in microfiche image storage is that of wear on the microfiche carriers, which degrades image quality, due to being kicked into and out of the display position. In the existing machine issuance of a valid microfiche carrier number results in withdrawal of the previously selected carrier and insertion of the carrier specified in the selection command, even when another microfiche image on the previously selected carrier is chosen. To prevent unnecessary wear, the controller's design had to include a method of aborting this carrier movement process whenever the next selected image was on the same car-

rier. Consequently, when the microfiche carrier number is defined as "88," the microfiche carrier movement process is aborted, and only the image row and column identifiers are processed.

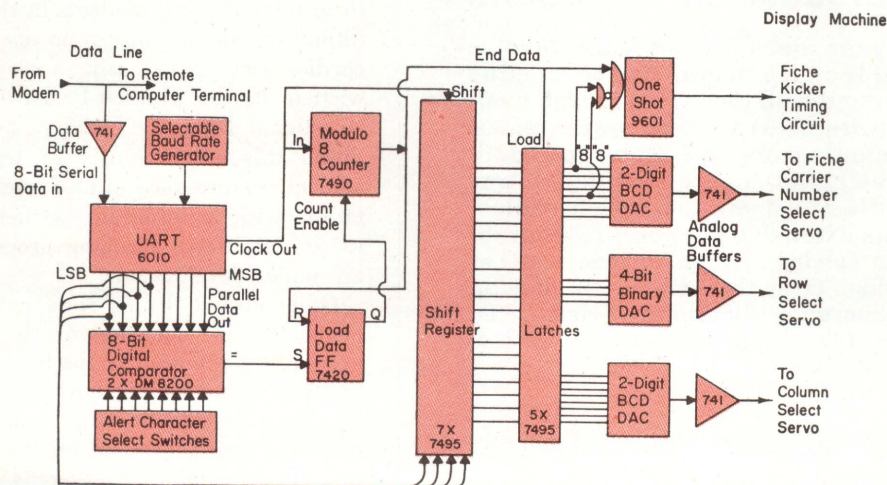
Controller Principles

The controller design resolved into a digital system (see Figure) for picking up 8-bit characters from the transmitted ASCII data stream, generating three analog voltages for driving the servomechanisms, and developing a signal to suppress the kicker if the next selected image is located on the microfiche carrier already in the display position. A nonprinting alert character in the ASCII data stream notifies the controller that the subsequent ASCII 8-bit serial characters will define the microfiche carrier number, image row, and image column selection. The microfiche display command has the general format of "A,XX,Y,ZZ," where A is the alert character, XX is the microfiche carrier number (one to 30), Y is the image row (one to five), and ZZ is the image column (one to 12). The alert character is chosen as one which is unlikely to be present in the data stream. Control K (Kc), the nonprinting character generated when a

K is typed with the control key held down, is used in this application.

The ASCII serial data stream is buffered and fed to a UART (universal asynchronous receiver transmitter). Baud rate and stop-bit format for the UART are selected to match the associated remote computer terminal. In the receiver (serial-to-parallel conversion) register of the UART, the ASCII character is successively compared with the alert character, as defined by switch settings, in an 8-bit digital comparator. The four least significant bits of the UART receiver register are also loaded into a shift register by the clock output of the UART. When the alert character is detected by the digital comparator, a load data flip-flop is set which enables a modulo-8 counter. At the end of the count of eight, the contents of those shift register flip-flops which contain alphanumeric data are gated into latches. Thus, the lower four bits of the eight ASCII characters that followed the alert character are detected and latched.

An end data pulse at the completion of the count of eight resets the load data flip-flop, and drives a one-shot circuit, initiating the timing sequence of the microfiche carrier selection process for the display machine. This one-shot is disabled if the microfiche carrier number is 88.



Block diagram of microfiche digital controller. Serial data transmitted from modem to remote computer terminal are picked up and converted to parallel data format by UART. Digital comparator detects nonprinting alert character and sets load data flip-flop. Succeeding characters, which define microfiche image selection, are loaded into shift register. After latching, register contents are applied to three DACs to produce three analog voltages, driving servomechanisms in display machine to show selected microfiche image

Digital outputs of the latches are connected to three digital-to-analog converters (DACs). Analog buffer amplifiers with preset gains and offsets generate the three appropriate servodrive voltages for the microfiche display machine. These amplifiers have bounded outputs to prevent servomechanisms from being driven off scale if an invalid digital number is set in the latches.

Circuitry is constructed on four 4.5 x 6-in (11.43 x 15.24-cm) circuit cards housed together with power

supplies in a separate 12 x 7 x 6-in (30.48 x 17.78 x 15.24-cm) case. A single front panel control switches from manual to computer fiche selection.

Applications

Any software system that can issue print commands with a format appropriate for microfiche selection is compatible with the controller. A zero must precede a microfiche carrier or an image column number

code of less than ten. A test routine should be included in a driver program to detect whether another image on the microfiche carrier currently in the machine display position is selected and, if true, 88 should be substituted for the microfiche carrier number code in the selection command.

Applications requiring computer-controlled display of a selection of a large library of hard data are appropriate for the system. Selection and display of microfiche images are considerably faster than display of alphanumeric data from computer storage at typical modem transmission rates. In other applications where a large static library of line diagrams is needed for CAI, microfiche storage has advantages of access speed and computer storage economy over graphic display methods.

The principle of using an alert character in an ASCII data stream to initiate a hardware function that is ancillary to a remote computer terminal could have applications in other examples; it could be used for limited digital or DAC input/output, or to switch the data stream from a cathode-ray tube (CRT) display to hardcopy terminal. Such systems do not require mainframe modifications, additional data lines, or special software facilities, and can be implemented with a moderate component cost.

Summary

The microfiche control system is currently being used with great success to instruct medical students in recognition of abnormalities on electrocardiograms (EKGs) using a program written in the Hewlett-Packard Instructional Dialogue Facility. In addition, this system is used for testing student performance in EKG interpretation with a program written in BASIC. Additional teaching programs are under development.

Other circuit details were not implemented in this design. A gate, driven by the output of the load data flip-flop, could be used to interrupt the data stream to the computer terminal during the acquisition of microfiche commands, thereby suppressing readout of these data at the terminal. The use of another alert character to cause a magazine eject under program control has also been considered. □



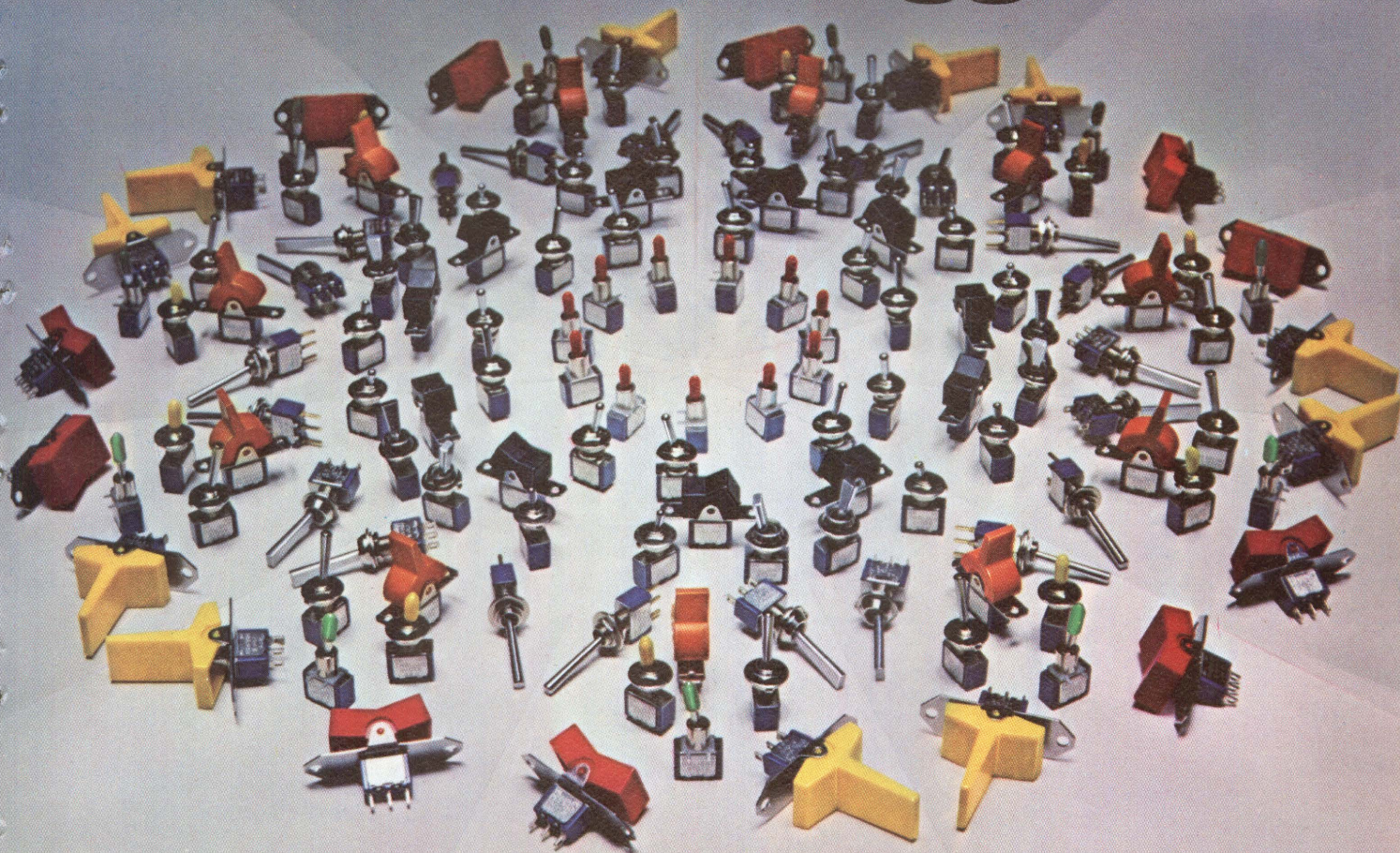
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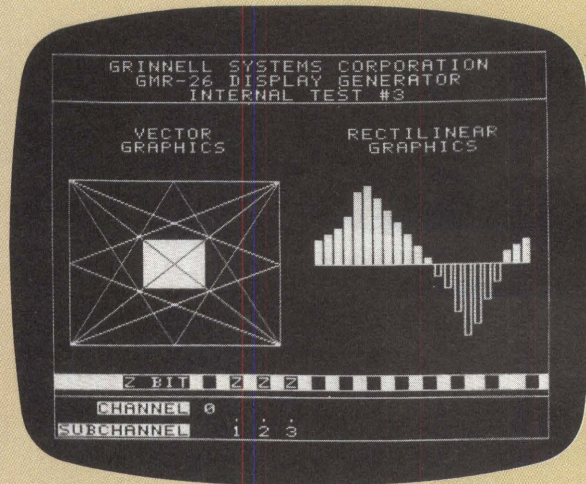
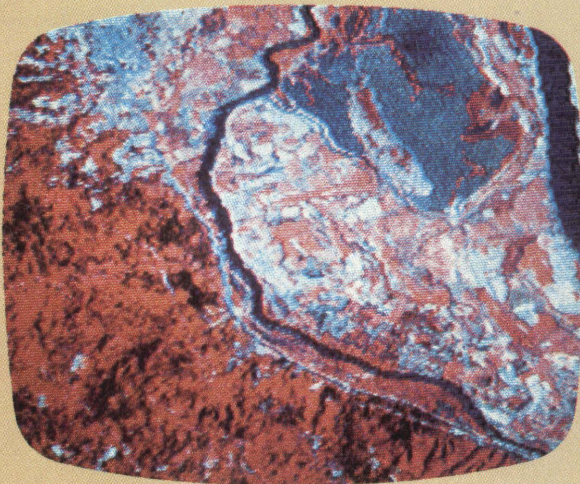
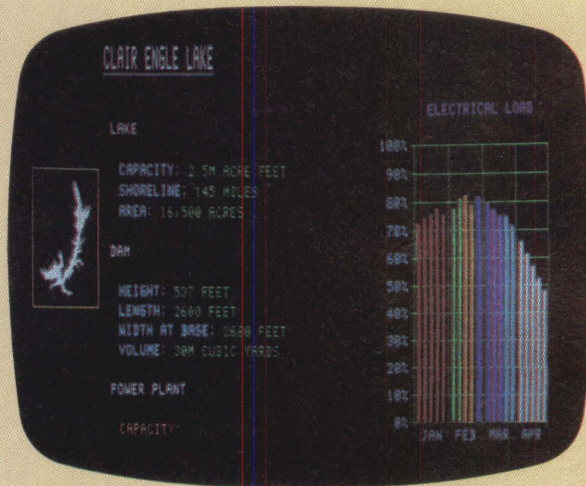
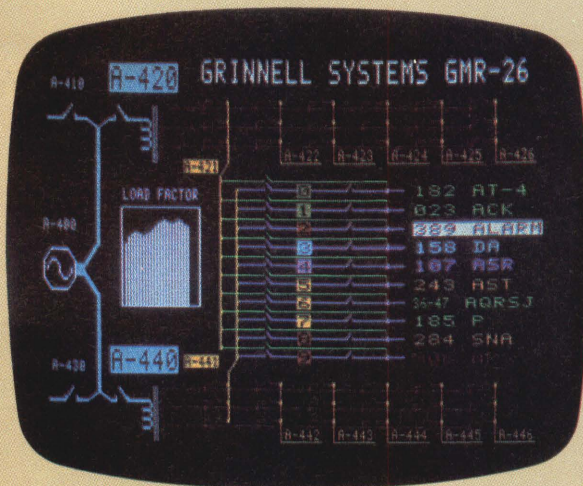
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Digital Image Processor Links TV Signal Sources to Computer

Roger Dahlberg

Quantex Corporation
Sunnyvale, California

Acquisition and modification of real-time video images for monitor display are achieved with a digital system, evolved on a block-diagram level, which is capable of coupling TV signal sources to a computer for fast data analysis

Image signals from standard television sources are now being computer-processed for fast data enhancement and analysis. These image sources, such as thermal cameras, low light-level cameras, and scanning electron microscopes, are finding increasing usage in diverse scientific and industrial applications, ranging from human cancer screening to material x-ray inspection.

A digital image interface, which couples the television (TV) signal source to the computer with simple noise reducing and contrast enhancing algorithms, is examined on a block-diagram level for economical implementation; microprocessor control of the interface is also explored. A video memory architecture is capable of real-time TV in, TV out, and random access, all transparent to one another.

Real-Time System Requirements

The interface system needed to link the image sensor to the computer must provide an analog-to-digital converter (ADC), a means of viewing the image in process, a video memory, a timing and control function, and a digital-to-analog converter (DAC) (see Fig 1). It should also offer noise reduction and a measure of real-time picture element (pixel) manipulation to reduce the computer's processing load. Certain simple arithmetic operations involving addition, subtraction, and shifting can be implemented easily in hardware at real-time TV rates to save computer power for non-realtime spatial image problems. In addition, the interface system should furnish storage of a video frame to facilitate transient image/event capture and recursive frame-to-frame real-time comparisons.

To further characterize system requirements, the typical composite video signal is examined. Although there are variants, the most commonly used TV standards involve a horizontal 525-line picture composed of two vertically interlaced field scans occurring at a 60-Hz rate. Sync pulses are embedded in the analog video waveform to define the beginning of each horizontal scan line and each vertical field scan. Most TV signal sources provide composite sync; thus, the digital image interface should be capable of extracting sync from the composite video waveform and using it to synchronize system operations. The A-D sampling clock must be synchronized to less than one pixel time with the horizontal scans to prevent sample jitter. Basically, sampling frequency should be determined by the bandpass of the

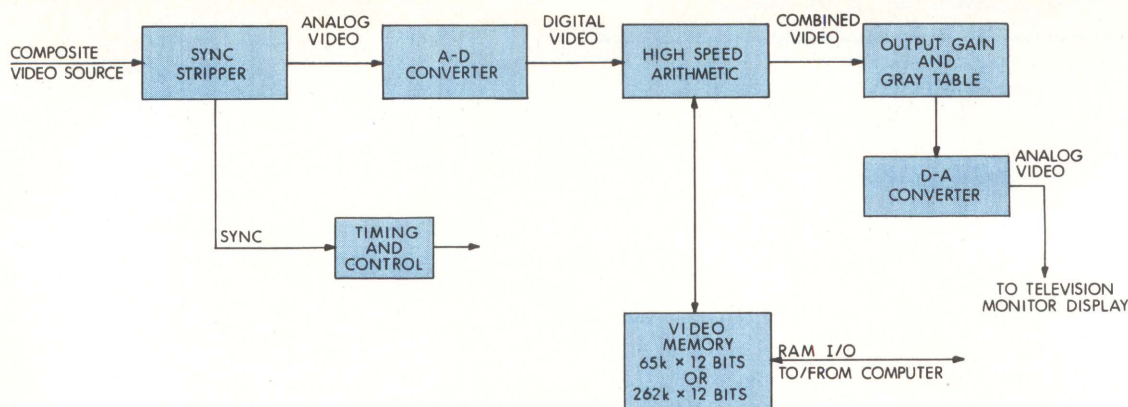


Fig 1 Digital image interface system. Composite video enters sync stripper where timing signals are extracted and sent to timing and control. Remaining analog video is passed through ADC into high speed arithmetic, where it is combined with digital video from memory. As memory video is read, it is simultaneously passed through gray table and DAC for display on standard TV monitor

video signal; however, it is usually more practical to determine this frequency from video memory dimensions that are integral powers of two. Memory dimensions of 512 by 512 and 256 by 256 are two practical choices, the former achieving higher resolution at the expense of more memory. These two sizes yield 10- and 5-MHz sample rates, respectively.

Another system characteristic to be considered is output gain. Since video memory might have more bits per pixel (shades of gray) than the DAC or display can accommodate, means must be provided for selecting the appropriate subgroup of bits for display. At this point in the system it is also convenient to provide digital expansion or compression of

selected amplitude bands for visual display on a TV monitor. This is readily achieved with a lookup table having alterable contents so that any reasonable transfer function can be obtained.

High Speed Arithmetic

Simple arithmetic functions can be performed at TV rates (10 MHz) that

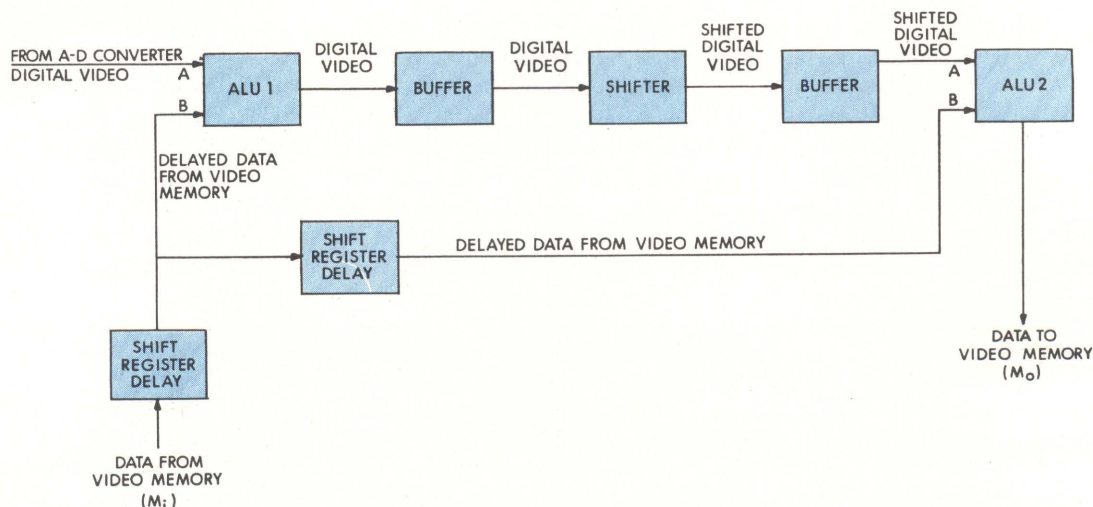


Fig 2 High speed arithmetic unit. Data from memory in TV sequential addresses are delayed and applied to ALU 1 along with A-D video. Results are buffered, run through shifter for arithmetic division by powers of two, buffered again, and then applied to ALU 2 as input A. Memory data are also applied to ALU 2 as input B, delayed further to align with shifter data. Results from ALU 2 are returned to video memory for display for further processing



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enhance or condition the video images provided by the TV source; these functions include summing, averaging, and differencing sequential incoming frames. The selected high speed arithmetic function operates on pixels as they stream in from the ADC, combines them with corresponding pixels from the image in memory, and stores the result back in memory for display and further processing.

High speed arithmetic units are shown in Fig 2. Sequential memory address generation is performed by a counter in the timing and control section. Shift registers in the data path from video memory to the arithmetic units provide alignment delays so that output video is time-registered with incoming video. This delay feature prevents an annoying one or two pixel shift in the image position within the TV raster when switched between analog and digital output video.

Two arithmetic logic units (ALUs) and a single shifter perform the required data operations. To sum corresponding elements in sequential frames in order to build signal amplitude and reduce noise, ALU 1 performs the sum, the shifter passes data without shifting, and ALU 2 passes its "A" input unchanged. Thus, video memory accumulates the

sum of sequential frames. If allowed to continue indefinitely, the sum eventually would overflow memory; therefore, control is provided for two stop conditions, either a fixed frame count or any pixel going to all ones.

To average sequential frames, the high speed arithmetic units perform the operation

$$M_o \leftarrow \left(\frac{V - M_i}{N} \right) + M_i$$

in which M_i is data from video memory, M_o is data to video memory, V is incoming video, and N is the averaging parameter. The equation is easier to understand rearranged as follows:

$$M_o \leftarrow \left(\frac{1}{N} \right) \times V + \left(\frac{N-1}{N} \right) \times M_i$$

A fraction of the incoming video (V), determined by the value of N , is added to a complementary fraction of the video memory (M_i), and the results (M_o) are replaced in memory. Thus, the amplitude of the memory contents is constant, and the recursive averaging process is continuous over an indefinite number of incoming frames. N is chosen to be an integral power of two (1, 2, 4, 8, 16, etc) so that division by N can be implemented by right-shifting the dividend. Both ALUs and the shifter execute the averaging equation. ALU 1 subtracts M_i from V , the

result is right-shifted $\log_2 N$ places by the shifter, ALU 2 adds M_i back in, and the data result (M_o) is returned to video memory.

To difference the memory and incoming video, control logic sets ALU 1 to the subtract mode and the shifter to right-shift by one bit position. ALU 2 passes its A input straight through. The sign (most significant bit) of the result is inverted. Accordingly, the result is

$$\left(\frac{V - M_i}{2} \right) + 2^{11}$$

This makes optimum use of the 12-bit memory. Since the memory word is treated as an unsigned integer for display purposes, any negative result from the subtraction $V - M_i$ would seem to wrap around, giving an apparent discontinuity to the gray scale of the picture if the sign bit were not specially treated. Hence, the right-shift and 2^{11} offset ensure a unipolar result and, therefore, a rational image.

Noise Reduction

All high speed arithmetic functions are useful in noise reduction. Two kinds of noise inherent in the video signal are random noise due to the behavior of electrons in electro-optical devices and in video amplifiers, and fixed pattern noise due to spatial

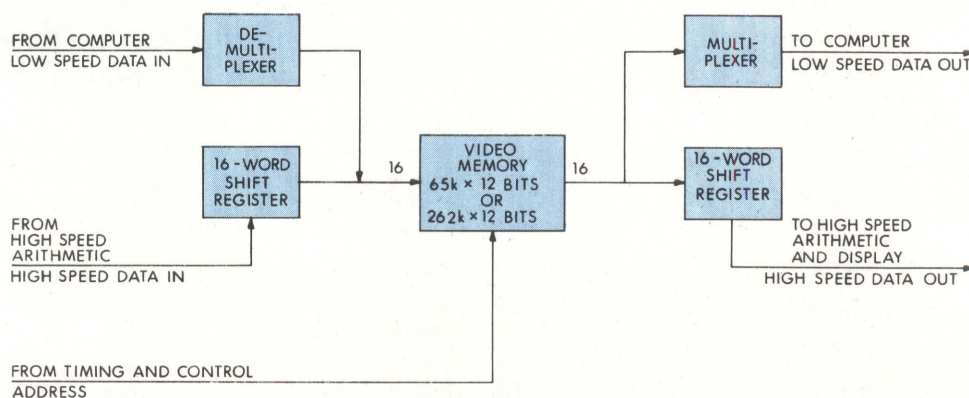


Fig 3 Memory organization. High speed data at TV rates are serially loaded into 16-word shift register. When 16 bits are assembled, data are simultaneously loaded into 16 memory chips. Similar process unloads high speed data for arithmetic computations and TV display. Low speed data are written into and read out of memory at random addresses during access cycles not used by high speed operations



“New cost/performance analyses made Inforex switch from in-house tape drive production to Digi-Data”

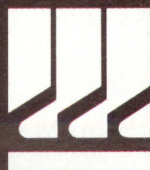
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imperfections in the video sensor—vidicon target blemishes, scan-related shading, and the like. Both summing and averaging functions provide signal-to-noise ratio improvement for random noise. Fixed-pattern noise can be eliminated by using the differencing arithmetic function. Initially, the fixed pattern is stored in video memory by recording a frame while the sensor lens is capped or light is otherwise inhibited. The fixed pattern plus the sensor noise are added; then, the memory contents are subtracted from the sum. Finally, the resulting fixed-pattern noise-free signal is stored in video memory.

Video Memory

Memory for the digital image interface has unusual requirements. It must provide simultaneous writes and reads at 10 MHz to service the incoming video and TV display monitor, and must also provide synchronous access for external devices, eg, computer input/output (I/O). The 10-MHz access is addressed sequentially with the sensor scanning sequence, and computer access is typically random in both time and address. For random access, external I/O argues strongly for random-access memory (RAM) instead of serial memory. The solution is an array of 4k or 16k dynamic metal-oxide semiconductor RAM chips, depending on whether the resolution is 256 by 256 or 512 by 512. Refresh requirements of the dynamic RAM are conveniently met by the constant TV I/O access to all addresses. Power consumption and cost are both reasonable. The block diagram for video memory is shown in Fig 3.

Bandwidth requirements for the 10-MHz TV access are achieved by serially assembling 16 pixels in a shift register and then loading all 16 in parallel into 16 memory chips. The reverse process reads out memory contents for high speed arithmetic and display. Sufficient spare time remains with this arrangement to allocate a RAM cycle for each 16-pixel TV memory cycle; hence, RAM cycles can occur transparent to the TV cycles, and the user can simultaneously acquire images, operate on them with a computer, and display results on a TV monitor. RAM access time for the computer is 1.6 μ s/pixel.

Microprocessor Control

Control of the digital image interface resides in a microprocessor programmed to interpret the control panel and external commands for the high speed arithmetic modes. Choice of a microprocessor for this seemingly simple task has implications beyond basic control tasks. Additional duties for the microprocessor include "learning" a control sequence from front panel key strokes, then repeating it on command; computing and loading the lookup table mentioned previously; and transferring images from memory to peripherals such as tape and disc drives.

Presence of the microprocessor also enables a user without a computer facility to have limited spatial image processing built into the digital image interface. The microprocessor has direct access to video memory for this purpose. The tradeoff for on-board versus offboard computation lies between the economics, limited speed, and utility of the microprocessor and the higher execution rates, peripheral resources, and expense of a general-purpose minicomputer. For an application involving small amounts of spatial pixel manipulation, such as a spectrograph or an industrial inspection device, the interface as a standalone unit is an economical choice. For use in acquiring images for extensive analysis, as in medical research, it serves as a noise reducing link between the video source and computer, where operations like contour plotting, spatial filtering, and area calculations can be performed efficiently.

Summary

A digital interface system between any TV signal source and a computer is designed to perform a limited set of image acquisition tasks at video rates—tasks which are performed economically in a "wired" computer but not in a general-purpose one. The system concept allows the user to implement an image processor with limited cost and later to add a general-purpose computer for more powerful image processing, using the initial increment of equipment as an interface system. A special feature of the system is its ability to simultaneously acquire, process, and display real-time video images. □

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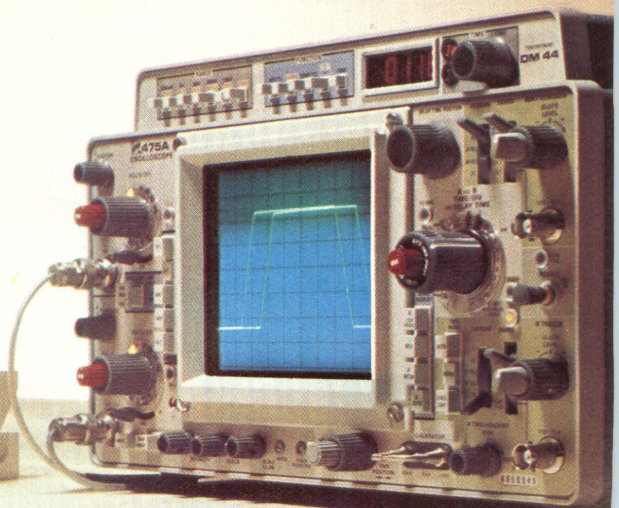
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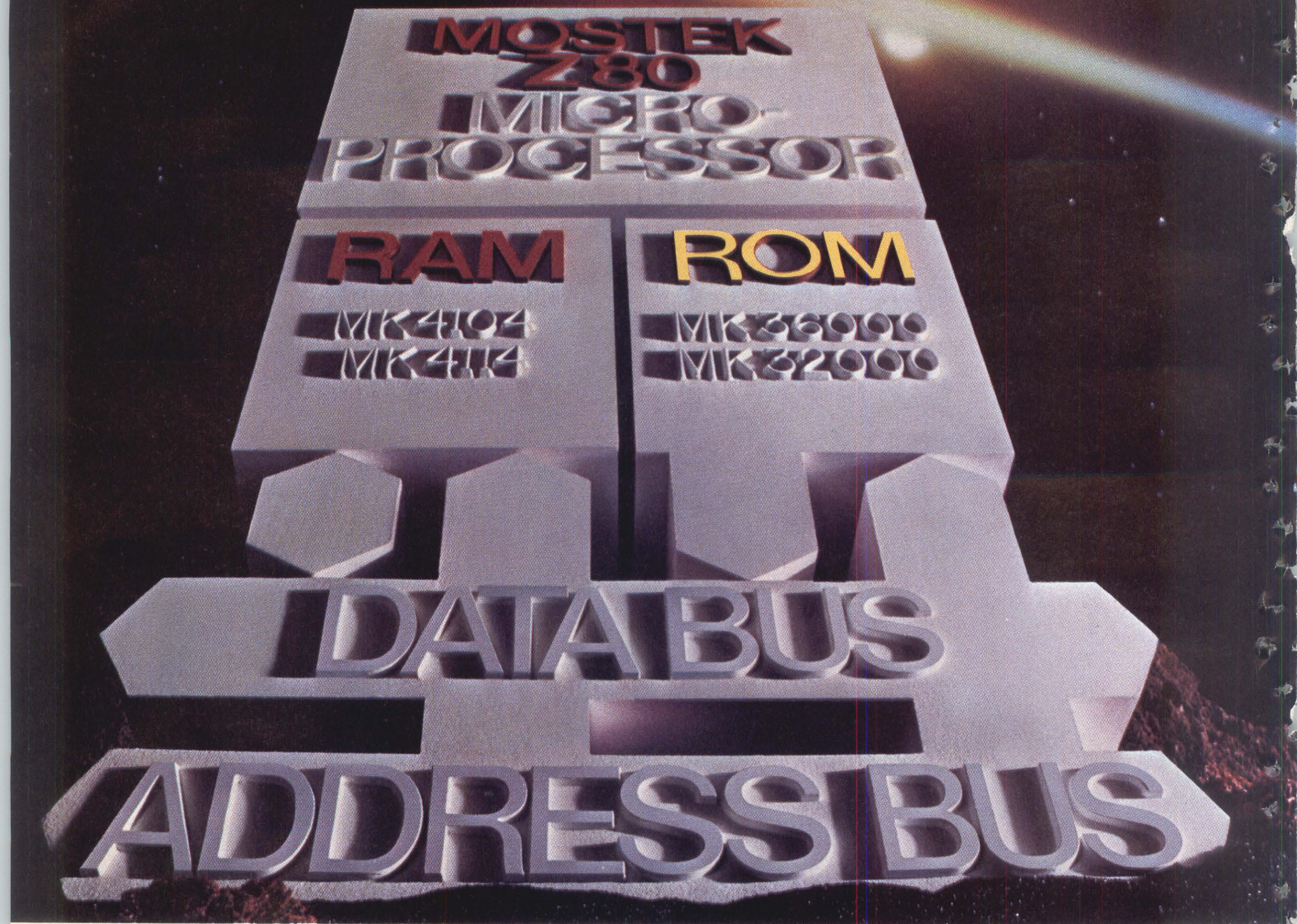
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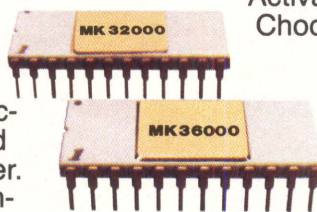
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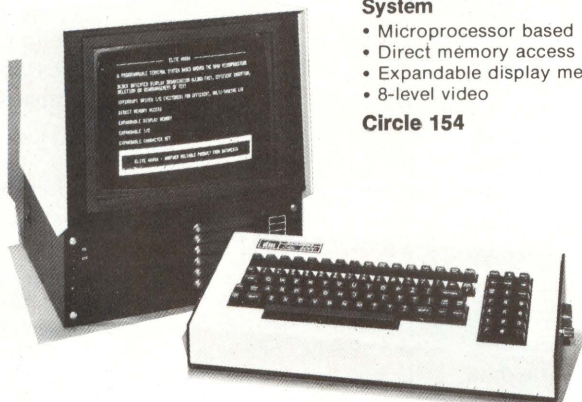
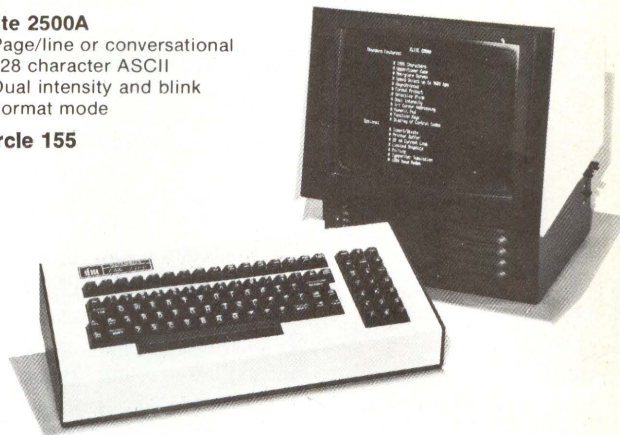


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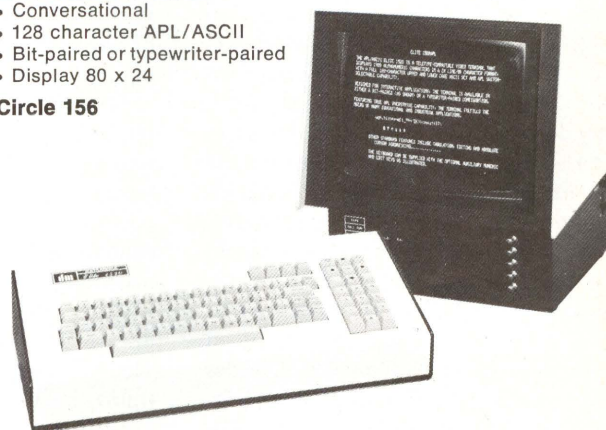


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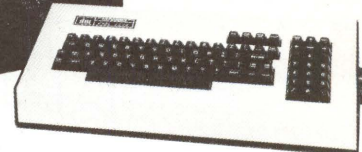
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Manchester Transition Tracking Loop

Improved synchronizer for biphas-L data

A symbol synchronizer optimized for Manchester-coded (biphase-L) digital data is used to lock the receiver onto incoming binary codes in the proper time sequence. The synchronizer is a special purpose computer which operates on sequential input samples of received data signals and is used to extract timing, data, and lock status information. Normally a digital transition tracking loop (DTTL) performs this function with a nonreturn-to-zero (NRZ) input. However, when Manchester-encoded signals are used with DTTL decoders, the biphas-L signal crosses from a high to low value during the time interval of a single-bit symbol, and the DTTL may be unresponsive.

In the Manchester transition tracking loop (MTTL), a separate phase-detection algorithm is incorporated for acquisition; the programmed acquisition-to-track sequence includes automatic bandwidth switching. Digital signal processing minimizes disturbing transients in this switching scheme. Additionally, the MTTL system has the most effective phase-de-

tection signal-to-noise ratio (SNR) of any synchronizing processor. It can operate at any symbol rate by simply changing the master clock frequency; all system parameters, such as loop bandwidth and damping factor, remain constant.

Integration in the phase detector is performed over a narrow window centered at the estimated transition time. Resulting phase-error estimate is corrected for the sense (direction) of the data, which is determined in one of two manners.

If the transition over which the phase error was obtained occurs at mid-symbol, then a data-detection integration (matched to biphas-L) is performed over a full symbol time centers at that transition. A resultant decision of the data sense defines whether the phase-error sample is due to a rising or falling transition. The phase-error sample is then multiplied by 1 or -1 to remove the data dependency.

If the transition occurs between two symbols, then integrations are performed over full symbol times on

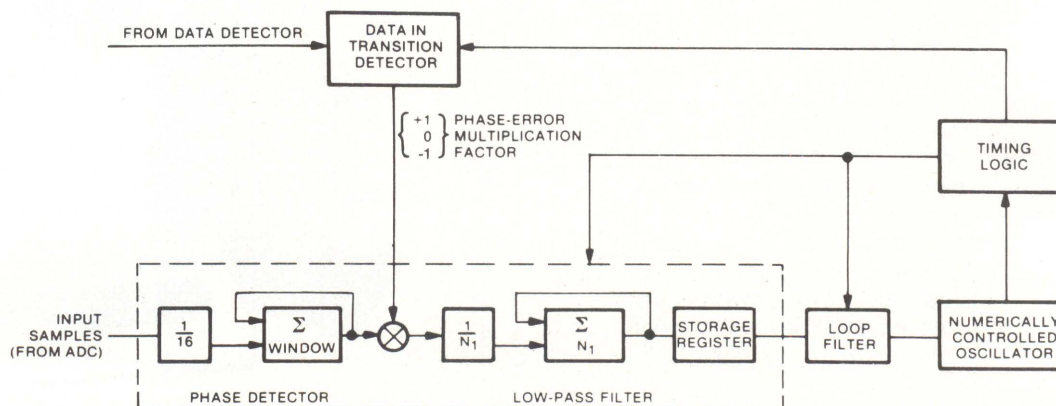
either side of the transition. Both integrations are compared with zero to determine the data estimates. Then the phase-error sample is multiplied by 1, -1, or 0 depending upon the direction or existence of the deduced transition. That is, a between-symbol transition is rising if two successive data bits are 1s, falling if 0s, and nonexistent for the two other cases of 10 or 01.

All decisions in the data-aiding portion of the standard DTTL are made via integrations performed over a full symbol time. Results are 3 dB better than existing designs which integrate over half-symbol times. Unlike the DTTL, the MTTL phase detector fully utilizes the additional half-symbol information present in the biphas-L signal.

Note

This work was done by Alfred Cellier, Lit Ning Ma, and Douglas Clayton Huey of TRW, Inc for Johnson Space Center. For further information, write to: John T. Wheeler, Technology Utilization Officer, Johnson Space Center, Code AT3, Houston, TX 77058. (MSC-14842).

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Phase detector for Manchester-coded signals performs signal integration over narrow window centered at estimated transition time. If transition occurs at mid-symbol, phase-error sample is multiplied by 1 or -1 to remove data dependency. Symbol synchronizer comprises receiver front end, data recovery, phase-detection, and clock-regeneration circuits. Input broadband SNR is processed by analog AGC circuit and then is sampled via a 4-bit parallel ADC. All subsequent processing is digital

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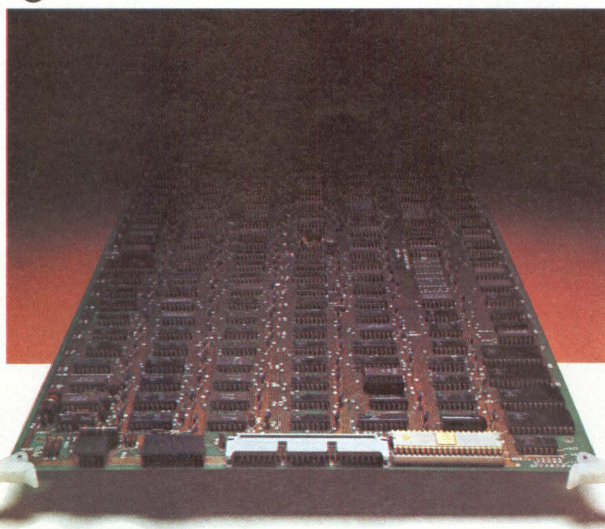
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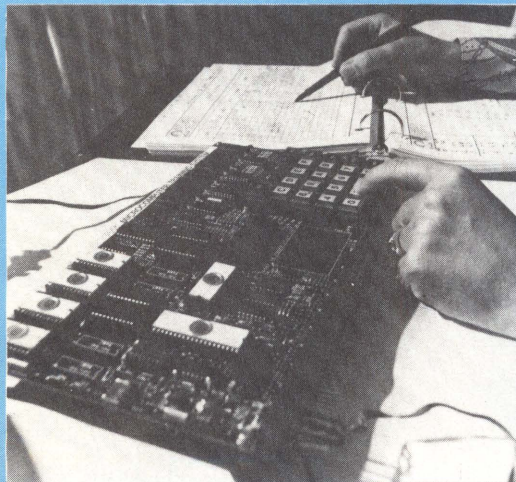
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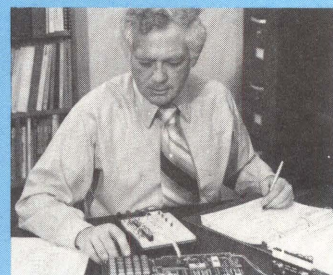
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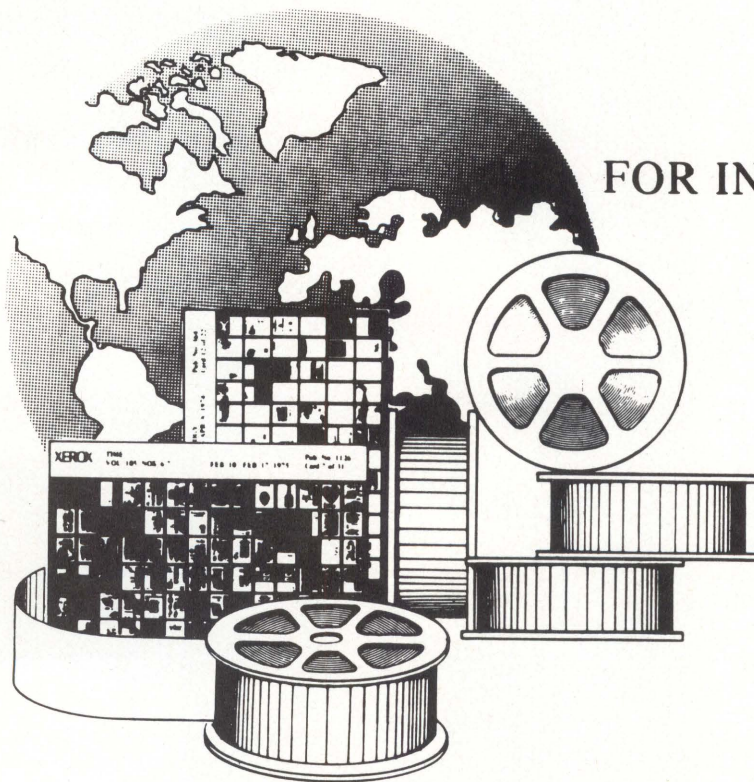


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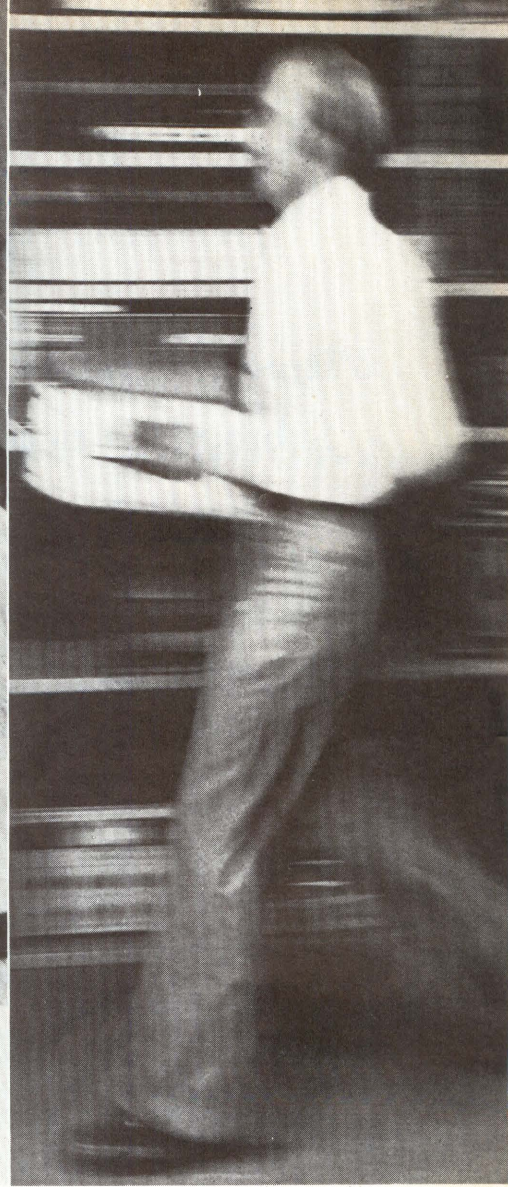
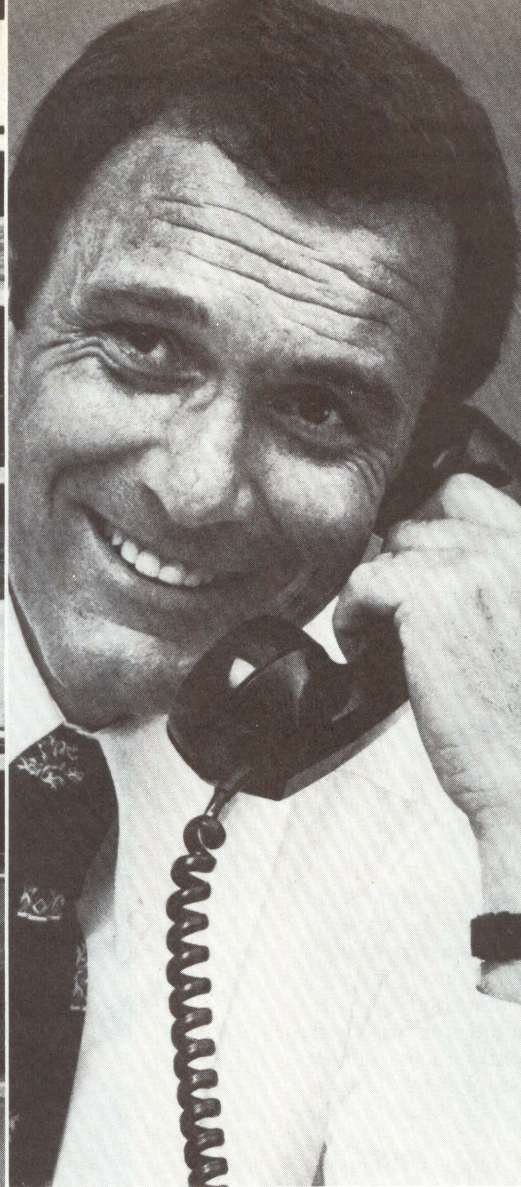


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Microcomputer Interfacing: Subroutines and Stacks

Peter R. Rony
David G. Larsen

Virginia Polytechnic Institute
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Jonathan A. Titus
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In previous columns, we have provided examples of short subprograms or subroutines that could be used by a main program. Subroutines, as powerful software building blocks, facilitate program development since they may be written and tested apart from the main body of software. In addition, they can be adapted for use with almost any type of program. This month, focus will be upon their operation as well as the use of stack instructions. Table 1 lists several definitions of terms to be covered.

Both unconditional and conditional jump instructions transfer computer control to another software task starting at the 16-bit address specified within the jump instruction itself. In many software tasks, however, short subprograms are used repeatedly. Examples of such tasks include mathematical computation, control, and teletypewriter input/output routines. Since it is wasteful to duplicate these subprograms throughout the main program, an attempt is made to separate them at the end of the main program and, in some manner, to branch to them when necessary.

Use of jump instructions to access these subprograms is unsuccessful since there is no link back to the main

Note: A 3-day "Microcomputer Interfacing Workshop" will be held on Dec 8-10 featuring the 8080 and 8085 microprocessors, with over 20 operating microcomputers available for participant use. Also scheduled is a 2-day workshop on Dec 6 and 7 entitled "Digital Electronics for Automation." Lectures and laboratory time with individual breadboarding sessions will focus on small- and medium-scale TTL ICs. Both sessions will be conducted by Dr Peter Rony, Dr Paul Field, and David Larsen at the Virginia Polytechnic Institute and State University campus in Blacksburg, Va. Further information is available from Dr Norris Bell, VPI & SU, Blacksburg, VA 24061, tel: (703) 951-6328.

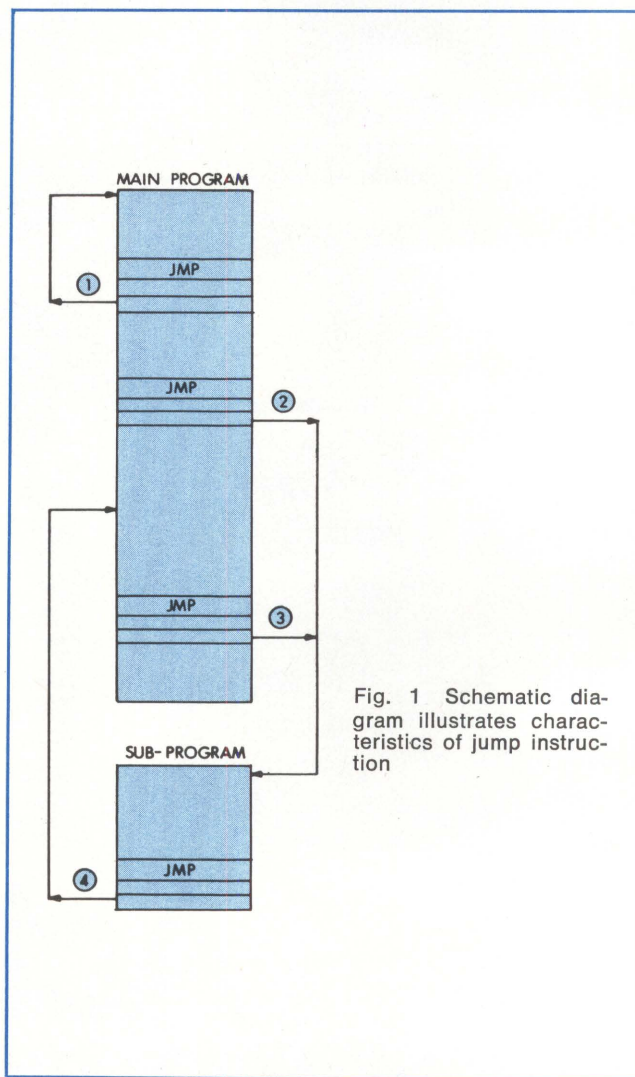


Fig. 1 Schematic diagram illustrates characteristics of jump instruction

program once the subprogram's task is completed. An additional jump instruction used at the end of the subprogram to point back to the main task is unsatisfactory because jump instructions are 1-way branches pointing to a single address (Fig 1). The jump instructions at 2 and 3 in this figure point to the same subprogram, but upon completion of the subprogram's task, the jump instruction at 4 can only provide a link to one place. Another operation, the call instruction, is required in order to insert the subprogram's software steps into the main program flow at points 2 and 3, without the problems associated with the jump instruction.

The call instruction, like the jump, transfers control to another portion of software; however, when that portion has completed its task, control is returned to the main program. In Fig 2, two subroutines are used by the main program, each being accessed by a call instruction which specifies the starting address of the subroutine as a 16-

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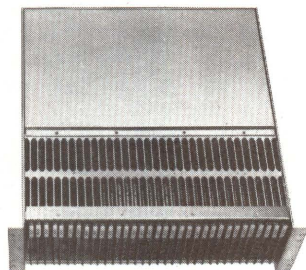
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TABLE 1

Software Terminology

Subprogram	A section of a program which may perform a particular operation to be used with a larger program. Subprograms are not general-purpose and usually are used by one program.
Subroutine	A general-purpose program which may be called or used by a main program or another subroutine.
Main Program	A short notation to indicate software tasks which occupy most of the computer's time.
Link	A pointer address which points the computer to another section of a program or back to a program which it may not currently be using.
Nesting	Operation of one subroutine within another, ie, a 1-min delay subroutine may call a 1-s delay subroutine 60 times.

003 000 061	START,	*003 000 LXISP	/Symbolic address of START
003 001 377		377	
003 002 003		003	
003 003 333	LOOP,	IN	/Input data from port 5
003 004 005		005	
003 005 376		CPI	/Compare it to 026
003 006 026		026	
003 007 312		JZ	/If it matches, go to DETECT
003 010 015		DETECT	
003 011 003		0	
003 012 303		JMP	/If it doesn't match, go to
003 013 003		LOOP	/LOOP and check again
003 014 003		0	
003 015 171	DETECT,	MOVAC	
003 016 323		OUT	
003 017 007		007	
003 020 166		HLT	

TABLE 2
Software Example
of Typical Assembler Output

bit, or 2-byte, word. Upon completion of the subroutine, control is returned to the next instruction that follows the 3-byte call instruction. Through the use of call instructions, the program shown in Fig 2 has inserted the subroutine program steps into the flow of the main software task. Subroutine No 2 is used only once, but Subroutine No 1 has been used twice even though it is present only once in the microcomputer's memory.

Each subroutine is accessed via a call instruction and ends with a 1-byte return instruction, RET, which contains no address information, yet which acts to return control to the main program. The return of control takes place since the call instruction saves a linking, or return, address that acts to branch the computer back to the address of the instruction immediately following the 3-byte call. The return instruction causes the microcomputer to retrieve the address from storage and to use it as the link back to the main task.

The 16-bit return addresses associated with call instructions are stored in an area of read/write (R/W) memory called the stack. Transfer of address information to and from the stack during call and return operations is performed automatically by the 8080 microprocessor; thus, the microprocessor pushes the return address onto the stack during execution of a call and pops it off the stack during a return. The actual memory area set aside for the stack is determined by the programmer through the use of an LXISP instruction, which loads the 16-bit starting address of the stack into the stack pointer register located within the microprocessor. It is the programmer's responsibility to set up a stack pointer before calls and returns are used, and to make certain that the stack area will not be used for other purposes during program execution.

In the program example shown in Table 2, we decided that the stack should have a starting address of 003 377. The first step in the main program, therefore, is to set the stack pointer to this address using the LXISP instruction. Later, when a call instruction is executed, the microprocessor transfers the return address to the stack area of R/W memory. If the stack pointer is initially set at address

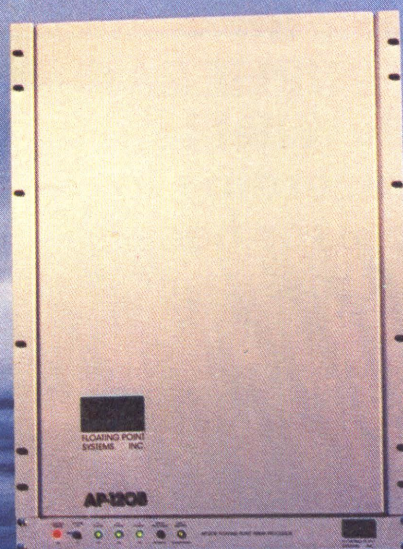
X, the return address is stored with the low address byte in location X-2 and the high address byte in location X-1. Thus, the stack adds address data at addresses below the address value of the stack pointer. When the return address is popped back into the microprocessor, the stack pointer is automatically incremented back to address X as the return address is retrieved byte by byte. When the next subroutine is called, the same stack locations are used for storage of the new return address since the old one has already been popped back into the microprocessor.

Subroutines may be placed one within another, or nested, enabling one subroutine to call another. In this way, a control subroutine may, in turn, call a timer subroutine; when the timer subroutine has completed its task, it causes a return to the control subroutine. This requires two levels on the stack, or four R/W memory locations, since two full 16-bit return addresses must be maintained on the stack while the timer subroutine is in operation. These are the return address for the timer-to-control link, and the return address for the control-to-main-task link. Stack operations take place automatically whenever a call or return is executed. Call and return instructions may be either conditional or unconditional, but each subroutine must contain at least one return instruction.

The microprocessor contains seven 8-bit general-purpose registers—the accumulator (A), B, C, D, E, H, and L. In programs using subroutines, register conflicts may occur since the subroutine and main task may both require the use of a specific register. One solution is to choose another register, but this is not always possible, particularly when the A register and flags are involved. To avoid register conflicts, the stack may be used for temporary data storage. All internal microprocessor registers are pushed onto the stack and popped back into the microprocessor as needed. Data are stored and retrieved as register pairs, with register A and the flags forming a 2-byte word that is treated as a register pair.

The subroutine in Table 2 is a time-delay routine in which the flags and registers D, E, and A are stored on the stack. Upon completion of the subroutine, data

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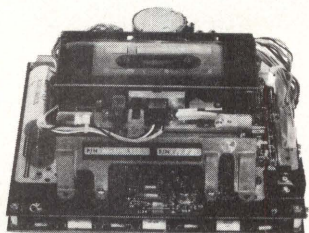
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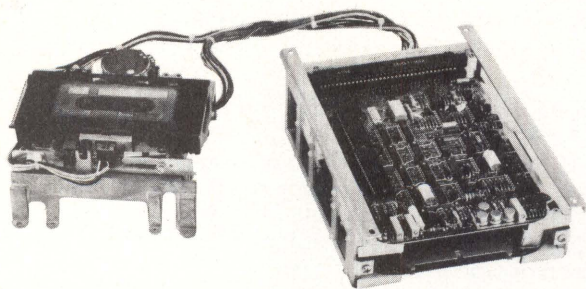
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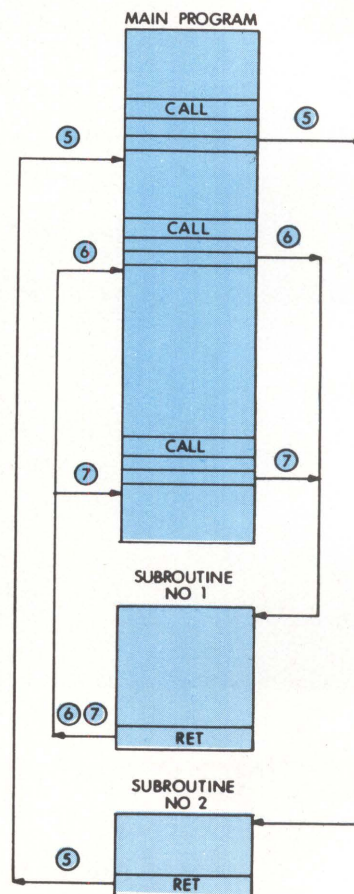


Fig 2 Characteristics of call and return instructions are shown

stored on the stack are retrieved and placed back in internal registers. The complementary operations of stack storage and retrieval are called push and pop, respectively. Notice that the stack pointer is initialized at the start of the program, before any other instructions are executed.

Use of subroutines in a program allows many complex tasks to be subdivided into small segments which are easy to link together and which relieve the problem of continuously rewriting common program steps and routines. A personal library of frequently used subroutines is indispensable when programming.

This article is based, with permission, on a column appearing in *American Laboratory* magazine.



TURNKEY 620 SYSTEMS FROM NEFF USING THE HP 9825 CALCULATOR.. the logical next step in data acquisition.

You're involved in a scientific, engineering, or industrial project that could use a high performance, low cost data acquisition system. But you know that system integration and software costs of most systems actually exceed the hardware. And your need is now, so you want a system that will take data immediately with minimum user training.

Our turnkey 620S was designed for you.....

620S is a sophisticated data acquisition system with amplifier-per-channel or differential multiplexer analog signal processing and using the H.P. 9825 computing calculator for system control, data analysis and recording.

Neff systems are known for high performance and the 620S is no exception. Consider 0.1% accuracy with 50kHz channel scanning rate, fullscale input sensitivities from 5 millivolts to 10 volts, up to 256 channels or 2048 channels fully expanded, and 120dB rejection of common mode voltages up to 300 volts. Selectable data filters, simultaneous sample and hold and input signal conditioning are but a few of the many available features.

The Hewlett-Packard 9825 calculator provides the 620S computer performance with the operating convenience of a calculator. Programming is simple with HPL, an easy to learn, high level language designed for scientists and engineers. Standard features include a live-keyboard, alpha numeric printer and cassette recorder. Up to 24K memory is available. Plug-in peripherals include floppy disk, line printer, x-y plotter, and tape punch. It also attaches to H.P. Interface Buss.

A complete, integrated data acquisition system thats easy to use — thats our turnkey 620S.

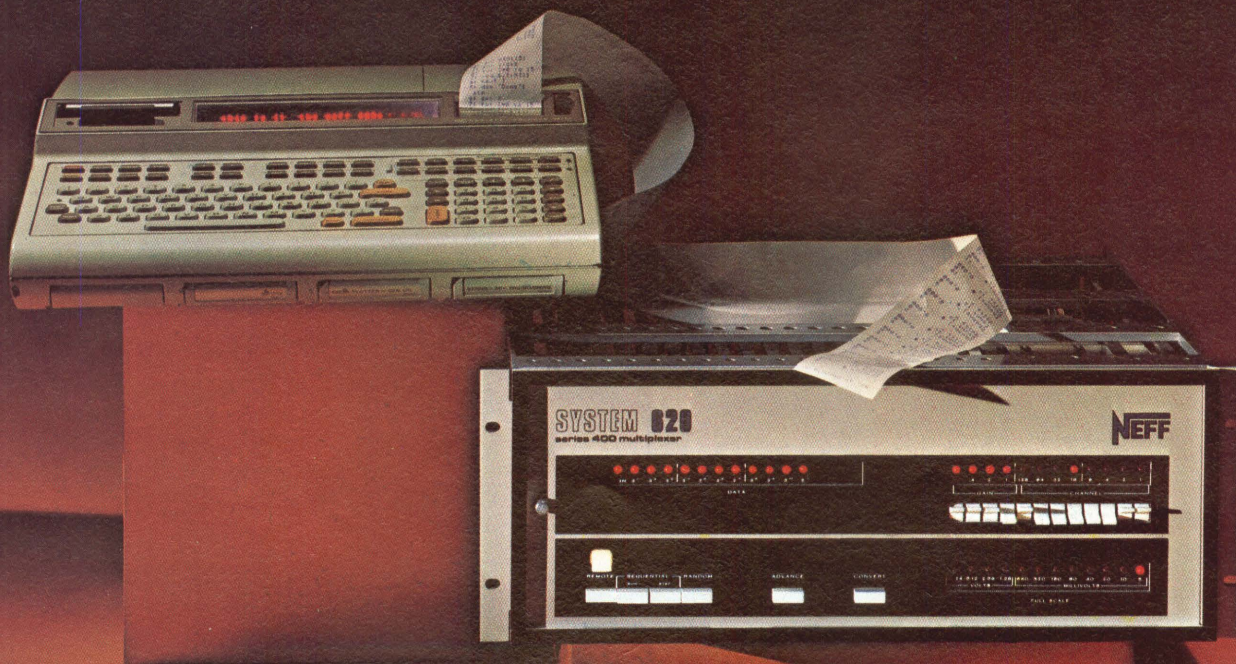
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CIRCLE 79 ON INQUIRY CARD



Universal Peripheral Control Components Boost Microprocessor Throughput and Lower Microcomputer Costs

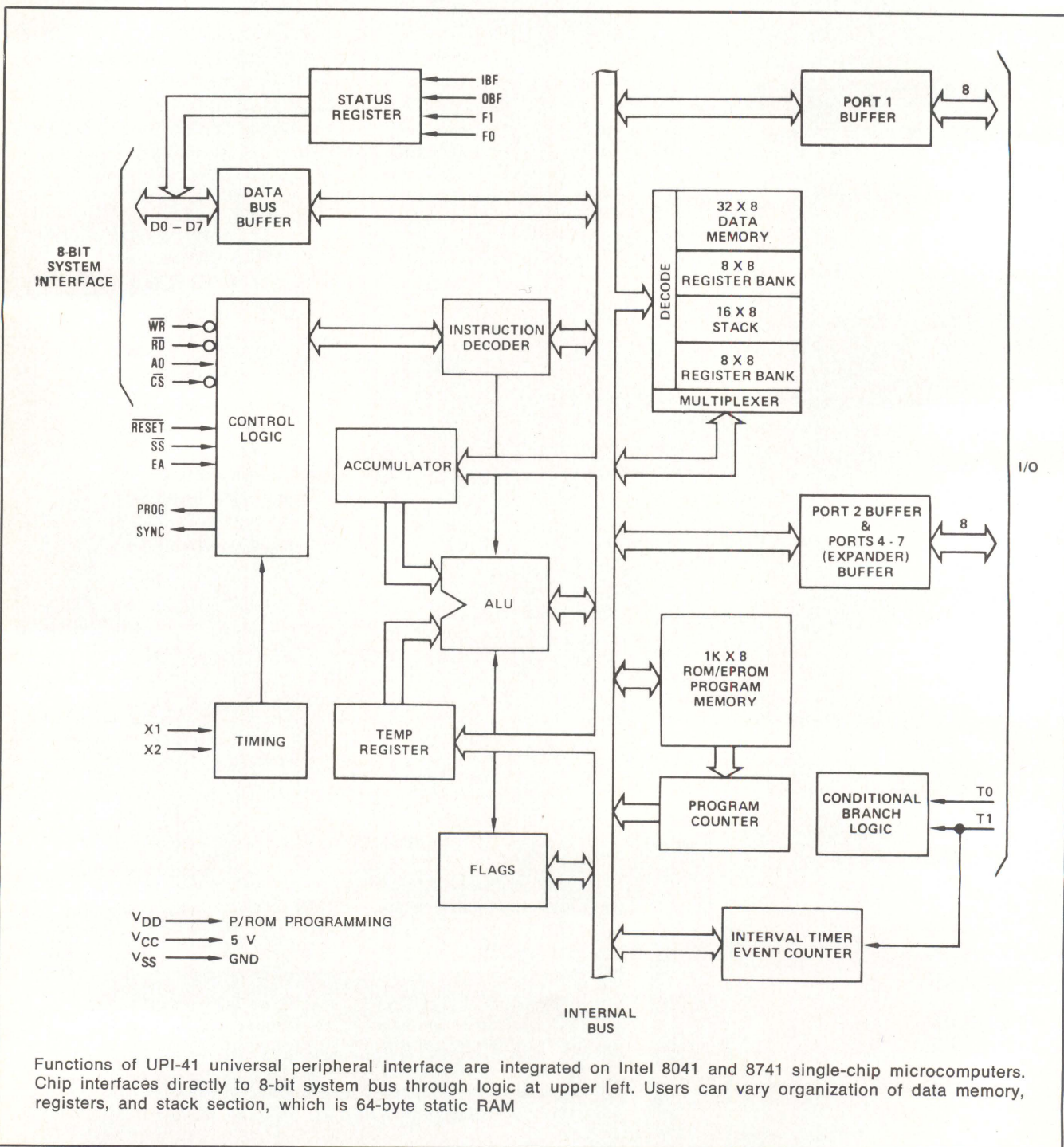
A group of single-chip slave microcomputers, designed to be used in a multiprocessor organization as slave processors and peripheral controllers, are said by Intel Corp's Microcomputer Div, 3065 Bowers Ave,

Santa Clara, CA 95051 to increase processing power and control flexibility of 8-bit microprocessors such as the 8080A, 8085, and 8048. The UPI-41™ universal peripheral interface components are claimed to be

the first microcomputers with the architecture required to operate as a microprocessor's intelligent slaves.

The basic UPI-41 is offered in two interchangeable versions, along with a low cost input/output expander for either microcomputer. The 8041 contains a mask-programmed ROM for program storage, while the 8741 with EPROM expedites system development.

Each 8243 i/o expander unit adds 16 lines onto four lines of the resident i/o subsystem. Functioning individually as input or output under software control, the 16 lines are organized



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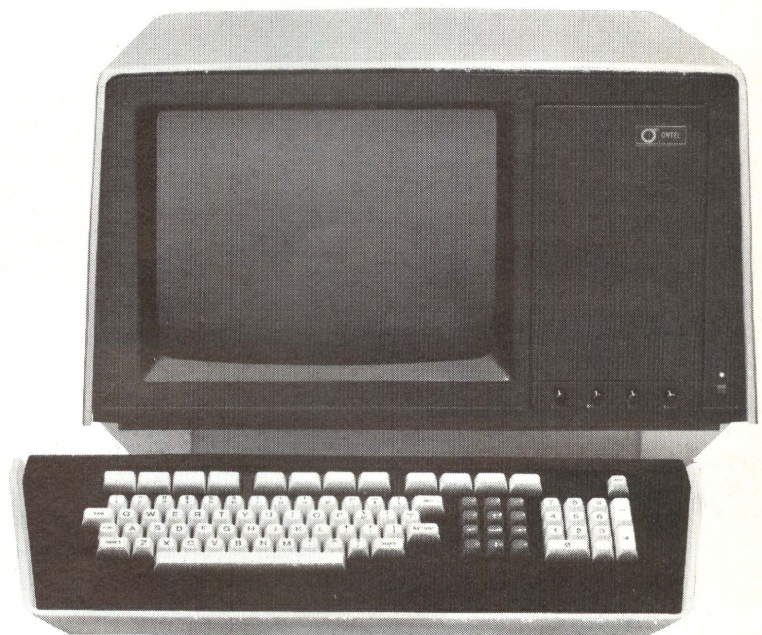
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National Sales Manager
Ontel Corporation
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as 4-bit programmable i/o ports. Multiple units expand i/o to over 100 lines.

The components are all fully user-programmable. Each slave contains a complete microcomputer integrated with a system bus interface, allowing a single microprocessor to communicate asynchronously with multiple slaves. The microcomputer contains an 8-bit CPU with a 90-instruction set comparable to the 8048's, 1k-byte ROM or EPROM, 64-byte static RAM for R/W data storage, programmable 18-line i/o subsystem, and two single-level vectored interrupts.

An internal oscillator and clock generate a 2.5- μ s instruction cycle and timing base for the 8-bit programmable interval timer/event counter which keeps track of elapsed time or counts events during program execution. It can also generate control timing sequences and communications baud rates. The 8041's power-down control feature allows data to be maintained during standby, keeping RAM alive while cutting power consumption by 85 to 90%.

An external slave bus configuration interfaces the chip directly to the system bus of most 8-bit processors. The logic built into the chip for this interfacing includes an 8-bit data bus buffer and 4-bit status register. Slaves transfer data with the master through the data buffer while the status register provides handshaking protocols required for 2-way communications via the system bus. This allows the master to communicate asynchronously with many slaves and allows the slaves and masters to operate at different clock rates.

All three units operate on a single 5-V power supply. The 8041 and 8741 are 40-pin devices and the 8243 is a 24-pin device.

Upgrading the single processor systems to multiprocessors with one or more intelligent peripheral controllers, the slaves unburden the master and simplify system software and hardware. Entire control algorithms can be stored in the microcomputer and executed in parallel with the main program.

In addition to interfacing and control functions, the slaves can handle data buffering and local data processing tasks. Each is a complete micro-

computer that fetches instructions from memory, reference memory, and i/o ports, and responds to interrupt and wait requests. The master can issue commands, transfer data at its convenience, and continue executing main programs. The slaves reduce costs of developing, manufacturing, and maintaining microcomputer systems, and simplify software development.

Primary applications are to interface and control printers, keyboards, displays, cassettes, A-D converters, serial data communications channels, consumer products, analog process control subsystems, and other peripheral equipment. Multiperipheral systems which normally require a microcomputer with several large random logic assemblies and a variety of LSI interface devices now can use additional chips. The microcomputers operate at ample speeds for electromechanical peripheral control. Serial data communications rates range to 9600 baud.

The 8741 with EPROM and single-step control facilitates program development. The chip may be reprogrammed to interface many types of peripherals. Between erasures, the memory is nonvolatile ROM.

Once programs are finalized, the 8041 ROM version provides a direct replacement with the added feature of low power standby. Both microcomputers are functionally equivalent and completely interchangeable, allowing the 8741 to be used for development and the 8041 for high volume production.

The components are supported by the Intellect[®] microcomputer development system for modular programming; it also has a universal p/ROM programmer. Intellect 888 system package has all software and hardware resources to develop programs in assembly language or PL/M. The ICE-41[™] in-circuit emulator offers symbolic debugging. Design manuals, training courses and workshops, and a user's program library are also offered.

The 8741 costs \$250 in single units and the i/o expander is \$8 for a single unit in a plastic package. The 8041 with RAM is mask-programmed; it is custom manufactured and will be sold directly to equipment manufacturers.

Circle 170 on Inquiry Card

8080 Hex Code Card Serves as Helpful Software Tool

This slide-rule-like aid for programming and debugging 8080 software is a 6.5 x 3" (16.5 x 7.6-cm) code card containing all mnemonics and corresponding hexadecimal codes. Color-coded instructions indicate which flags are affected during execution. Back of the card contains an ASCII code chart for all 128 characters plus 8080 status word and register pair codes. Tychon, Inc, PO Box 242, Blacksburg, VA 24060 is offering the card for \$2.95 postpaid. Circle 171 on Inquiry Card

PACE Microcomputer Disc Operating System Speeds Development

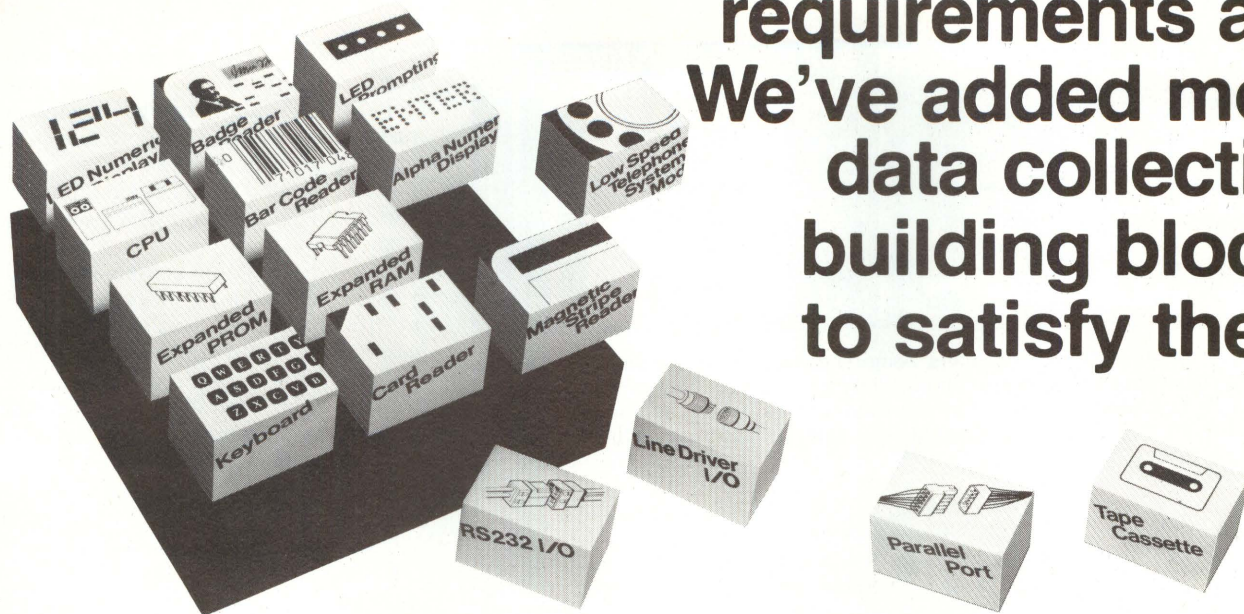
The combination of software and firmware—a monitor, comprehensive file manager, and file i/o subsystem—obtained from the IPC-16P/840 disc operating system (DOS) reduces the time required to assemble, edit, and execute microprocessor and microcomputer operating and application programs. The Microcomputer Systems Group of National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051 has equipped the system with a dual floppy disc drive in a standalone enclosure, interface circuit subsystem card, ROM card containing firmware, and complete operating software on a diskette.

Each drive holds a diskette which stores up to 158k words of unformatted data, with a maximum of 268 hexadecimal and 616 decimal sectors each. The interface card provides protocol for the dual disc drive and an optional user-supplied CRT terminal. The firmware card operates both disc mechanisms, formats data, and controls data transfers.

The system can be installed on any IPC-16P PACE microprocessor development system with 12k words of RAM and a heavy-duty power supply. Both cards are inserted in available slots in the system.

Other firmware handles data formatting and transfer between the PACE CPU and CRT terminal. i/o is

You tell us what your data collection requirements are. We've added more data collection building blocks to satisfy them.



EPIC DATA's Model 1647 data collection terminals and Model 1648 system control units (SCUs), let you configure exactly the data collection system you need. These "building blocks," based on microprocessor architecture and modularity, provide you with simple, practical and flexible terminals or systems for virtually any combination of requirements you may have.

simple. Building blocks can be combined to enable collection of information from a wide variety of pre-prepared and variable data with resulting improved efficiency and reduced errors. No computer knowledge is required for operation. Terminals can be programmed to: provide customized input, output and processing of data; prompt the user through entry steps and validating of data; and enable off-line or on-line operation.

EPIC DATA terminals are rugged, compact and lightweight. They can be wall-mounted or placed on a desk and are easily exchanged during maintenance.

practical. Environmental tests conducted in conformity with MIL-STD-810 plus in-depth, on-site testing assure reliable operation over a broad spectrum of hostile, industrial environments. Simple design and rigorous testing have resulted in an impressive MTBF.

flexible. EPIC DATA terminals can optically read punched badges and 80-column ANSI cards. User-defined keys are available for inputting variable data. Key entry data or time of day is displayed and LEDs are available for prompting.

Terminals can be configured to scan bar codes and magnetic stripes or accommodate other peripherals through RS232 ports. Display options include additional numeric displays, up to 15 LEDs for prompting and a 32-character alpha/numeric display. Serial asynchronous or synchronous communications ports with either RS232 or line driver I/O and a low speed modem may be added. Parallel communications ports are also available. Both PROM and RAM memories are expandable.

Newest Building Block: More to Come in Next Few Months

A self-contained cassette tape recorder providing up to 2.88 megabits of storage for transaction logging or store-and-forward applications is now available. The modular reel-drive tape recorder, like the rest of the building blocks, features high reliability and ease of maintenance. There is no pinch-roller or capstan to wear tape; only the head touches the tape.



SCUs. Model 1648 SCUs can be configured to poll up to 100 terminals, assemble transactions, format data, append time and date, and store or forward collected data to the host.

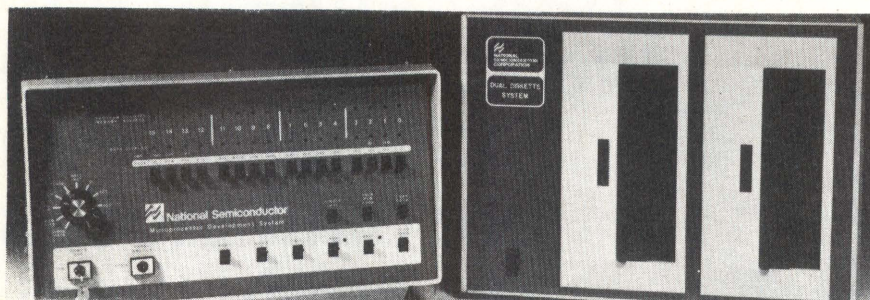
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Dual floppy disc operating system offers comprehensive file management capability, support for assembly programs, editors, linking loaders, utility programs, and diagnostics. It operates with National Semiconductor's PACE microprocessor development system to reduce development time, speed debug procedures, and simplify program testing

RS-232-compatible at rates of 300 or 1200 baud; a 20-mA current loop i/o with 110-baud rate is also available for teletypewriters.

The ROM resident monitor provides management control over system configuration and program execution. The dos file manager residing on diskette facilitates file maintenance, handles space allocation, and provides four levels of file protection. Symbolic naming of program and

data files is available. A collection of software routines for building programs is contained in the i/o file subsystem.

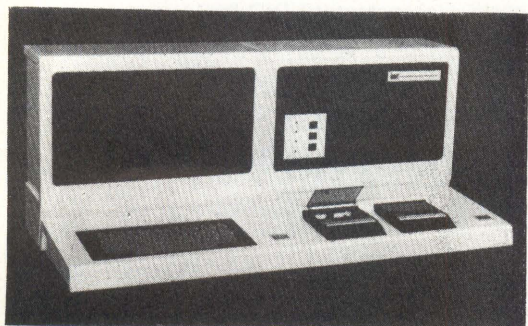
Other features include PACE assembler, DOS editor, linkage editor, p/ROM paper tape/punch utility, and disc patching utility. Price of \$4500 includes the dual floppy disc with electronics and power supply, p/ROM card for firmware routine, and disc/CRT interface card and cables.

Features of μ Computer Development System Simplify Design Tasks

Eliminating the need to be a programmer in order to implement a microcomputer system, the Micro-Command System™ features an integrated hardware/software package that supports development of either 8080 or Z80 microprocessors without changing the CPU. A Touch-Sense™ lightpen for interactive i/o permits a menu-oriented interactive software development process. This adds a 2-dimensional method of program

development, eliminates the problem of keyboard typing errors, and minimizes the list of commands that the designer needs.

Designed by Information Control Corp, 9610 Bellanca Ave, Los Angeles, CA 90045 to make the most often used components more convenient, the system also features an ASCII keyboard, 40 x 24 character set CRT, dual floppy disc (or optional dual cassette tape) storage system, and 16k to 64k bytes of static RAM with 512 to 2048 bytes of ROM which requires no address space restriction in RAM. An EPROM programmer, boot-



Lower cost option of micro-development system from Information Control Corp has dual cassette tape storage. Hardware/software package for 8080- or Z80-based systems, light pen for interactive i/o, and menu-oriented software comprise features. Standard version has dual floppy discs

strap loader in ROM, vectored interrupts, DMA, and a software package comprising editor/monitor/assembler programs complete the system. An optional In-Circuit-Debugger™ supports both 8080 and Z80 microprocessors with a common Z80 software base.

Standard desktop console-mounted version with floppy discs is priced at \$6950; optional version with dual cassettes is \$4875. They are compatible with a variety of printers through both parallel and RS-232 (serial) output ports.

Circle 172 on Inquiry Card

System and Support Facilitate Software/Hardware Development

The COSMAC Development System II (CDP18S005) is an interactive software and hardware prototyping system for product development. Based on the company's 1800 family of microprocessor parts, it uses the RCA1802 microprocessor as CPU and includes a RAM-based resident editor and assembler for fast program development. Additional space for i/o devices allows it to be used for hardware prototyping and evaluation. Accessories for the system include a micromonitor debugging tool, floppy disc system, and microterminal.

Comprising the system are a 19" (48-cm) rack-mountable chassis with PC backplane; internal power supplies, clock, and controls; a front panel with controls and display; and seven plug-in PC modules including CPU, control, address latch and bank select, 4k-byte RAM, ROM/RAM, i/o decode, and terminal interface. There are seven spare memory PC module positions and 10 spare i/o positions. Extra memory or optional i/o modules are available or may be user designed.

Standard 20-mA current loop and EIA RS-232-C interfacing are provided. All that is needed to make the system operational is the addition of a data terminal.

Both paper and magnetic tape cassette versions of the resident editor and assembler programs are offered; they can be loaded into the 4k-byte RAM. The utility program which is supplied allows the user to inspect and modify memory and to

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Four value-packed true line printers
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From \$3900 for the TermiNet 310 printer to \$5130
for the TermiNet 340 printer (user quantity 1).

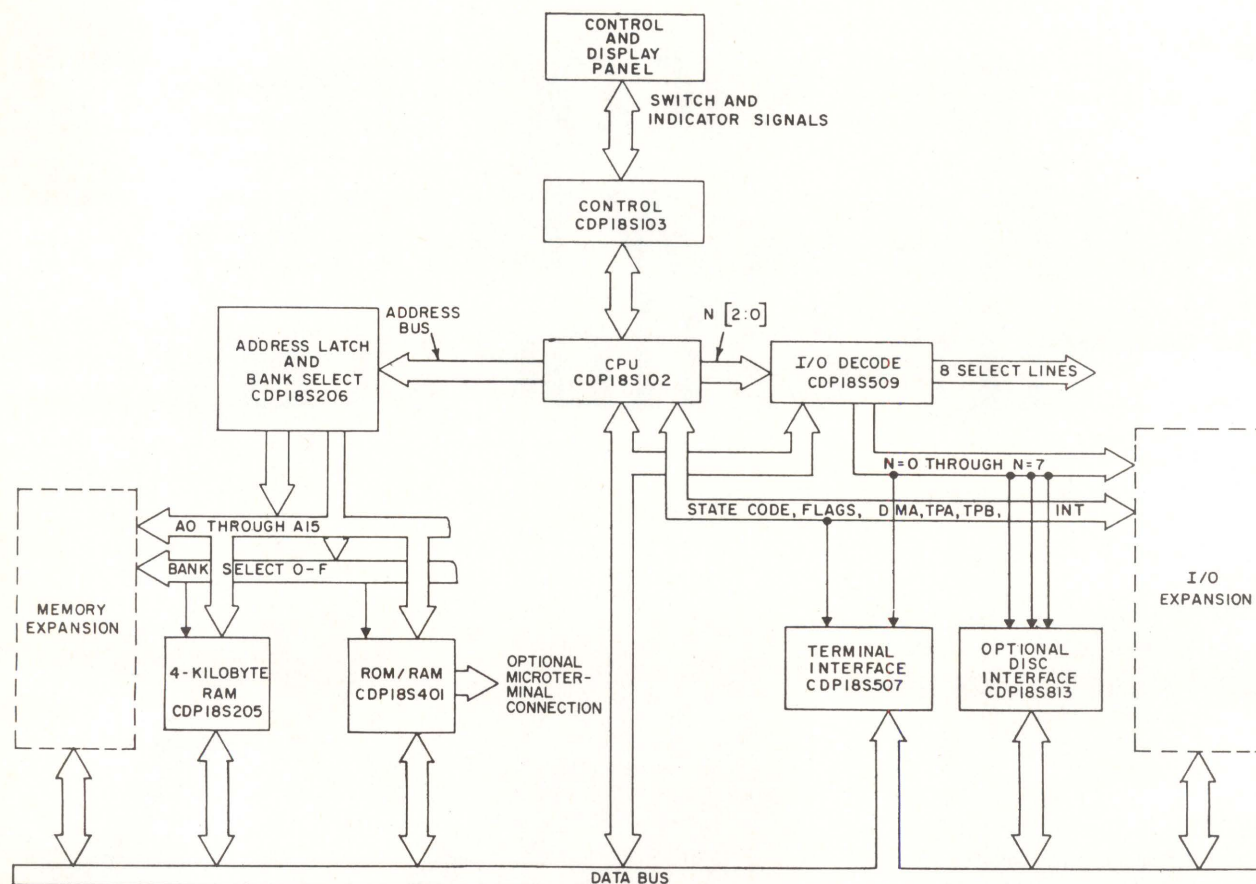
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For your special kind of needs—
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CIRCLE 82 ON INQUIRY CARD





Designed for flexibility and expansion with seven spare memory module and 10 spare I/O positions, RCA's COSMAC development system can be used for hardware prototyping as well as program development. In small volume applications, it can be major building block for dedicated microcomputers

start program execution at any location. It also provides the capability for program load, memory dump, and terminal interfacing for serial ASCII data terminals. It automatically adjusts to baud rates between 110 and 1200, and operates in full- and half-duplex mode.

RCA/Solid State Div, Box 3200, Somerville, NJ 08876 has introduced two optional accessories in conjunction with the development system. A mass-memory storage unit, the COSMAC Floppy Disc System II (CDP18S805) significantly reduces time necessary for microprocessor software assembly and editing compared with systems using other storage media. It includes a dual-disc drive mechanism, interfacing hardware, software for loading programs from the diskette into memory, and

special versions of the COSMAC resident editor, assembler, and utility programs.

Two versions include one designed for domestic use, operating on 115 V, 60 Hz, and one for overseas use, operating on 115 or 220 V, 50/60 Hz. The IBM-compatible diskette holds 256,256 bytes.

A low cost, low power, non-hard-copy alternative to conventional data terminals is the COSMAC Microterminal (CDP18S021) which controls a COSMAC microprocessor-based system, reading and modifying memory, and providing hexadecimal I/O capability. It features eight control functions.

Specifically suited for interfacing with the evaluation kit or development system, it can also be designed into user-built systems to provide control, communications, and de-

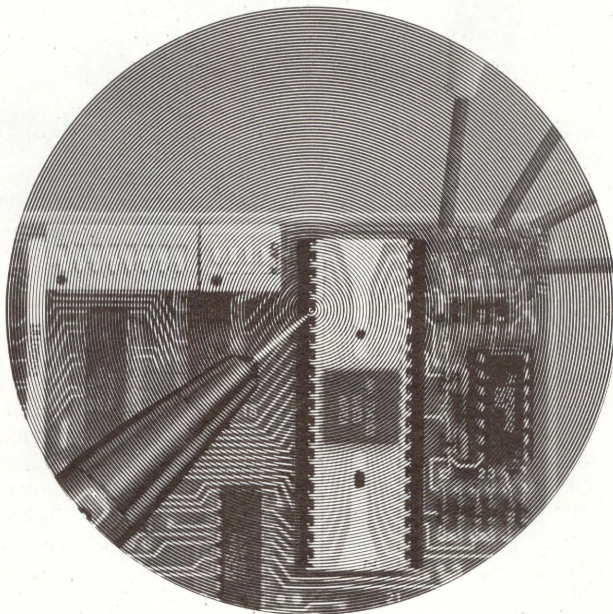
bugging functions. The compact terminal includes a hand-held keyboard and display unit of eight 7-segment LEDs, plus a cable and mating connector, and ROM containing a utility program (UT5). It requires less than 375 mA at 5 Vdc.

For microprocessor applications, a 600-mA, 5-V power supply (CDP18S023) is available to power both the Microterminal and evaluation kit augmented with 4k bytes of RAM. The supply operates directly from any standard 115-V, 50-/60-Hz outlet.

In single quantities, prices are \$2900 for the development system, \$3320 for the floppy disc system, \$180 for the microterminal, and \$25 for the microsupply. Instruction manuals are supplied with each unit.

Circle 173 on Inquiry Card

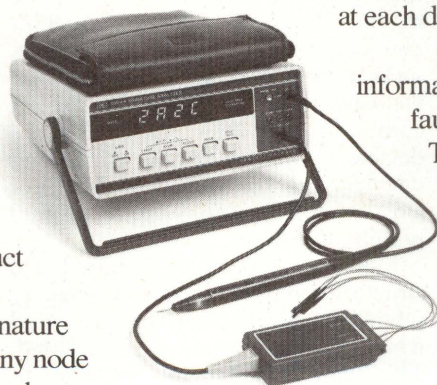
Troubleshoot microprocessor products fast—



right down to the component level.

Here's HP's new Signature Analyzer. It makes it economical to find the faulty component in a microprocessor-based product both in production and in the field. No longer is it necessary to make a large investment in expensive modules or boards for service. And no longer do you have to troubleshoot by conventional and costly hit-and-miss methods. It could even eliminate the need to partition your product for modular service.

The concept is simple. The 5004A Signature Analyzer converts lengthy bit streams at any node in a circuit into short, four-digit, hexadecimal



“signatures.” Just activate a digital exercise routine in the circuit under test, and compare the bit stream “signature” at each data node with the known good signatures previously written into your manual. This information lets you backtrace right down to the faulty component. Quickly and confidently.

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1507 Page Mill Road, Palo Alto, California 94304

Microcomputer System Adapts to Meet Specific OEM Needs

Suited to OEM systems and development work, the basic 16.175 x 6.875" (41.085 x 17.463-cm) single-board 90 MPS includes 6k bytes of memory (4k of dynamic RAM, 1k of static RAM, and 1k monitor with debug instructions in 2708 EPROM), two Z80 parallel i/o chips providing four parallel i/o ports, a UART with RS-232-C and 20-mA current loop interfaces, 2.5-MHz crystal clock, Z80 counter timer, and p/ROM programmer for 2708 type EPROMs. All i/o is via three 60-pin flat ribbon connectors, eliminating the need for motherboard and card cage assemblies.

Quay Corp, PO Box 386, Freehold, NJ 07728 also supplies the system with onboard expansion of dynamic RAM up to 16k bytes using 4k x 1 devices or up to 65k bytes using 16k x 1 devices. A total of 1k bytes of EPROM can be installed.

Sockets permit addition of two more Z80 PIO chips. An option for 4-MHz operation is also available. Basic system is priced at \$695 (quantity 1) and \$500 (OEM quantities 100).

Circle 174 on Inquiry Card

Ready-to-Use System Fits Small Business and Personal Computing Needs

The assembled TRS-80 microcomputer system consists of a 53-key ASCII keyboard and microcomputer, plus regulated power supply, data cassette recorder which is computer-controlled through an interface, and a 12" (30-cm) video display monitor. At the heart of the U.L. listed system is a Z80 8-bit microprocessor chip that serves as the CPU. Memory is 4k ROM and 4k dynamic RAM, internally expandable to 12k ROM and 16k RAM for a maximum of 62k.

Support includes instruction manuals, software programming (level 1 BASIC in ROM), firmware, and hardware. Prerecorded cassette programs are supplied for small business applications such as payroll, accounts receivable, and inventory control, as well as for educational purposes and



Containing a 53-key keyboard and Z80 microprocessor chip, Radio Shack's fully assembled TRS-80 microcomputer system has regulated power supply, video display, and data cassette recorder for small business, home, and educational use

home uses. Provisions allow for later addition of peripherals such as additional tape recorders, disc programming, and a hardcopy printer.

The portable microcomputer and keyboard from Radio Shack, div of Tandy Corp, 2617 W Seventh St, Fort Worth, TX 76107 measure 16.5

x 8 x 3.5" (41.9 x 20 x 8.9 cm); the display monitor measures 16.5 x 13.5 x 12" (41.9 x 34.3 x 30 cm). Price of the system with monitor and cassette recorder is \$599.95; the microcomputer alone sells for \$399.95.

Circle 175 on Inquiry Card

Large μ Computer Memory Aids Building of Systems for Industrial Control

A large onboard memory capacity of 17k and complete 8080A instruction set are highlights of the CCS-1143 single-board microcomputer developed by Control Logic, Inc, 9 Tech Circle, Natick, MA 01760. Contained on the single PC board are an 8-bit Z80 microcomputer, 1k x 8 RAM, sockets for up to 16k bytes of 2708 EPROMs, serial interface for 20-mA current loop or EIA RS-232-C serial devices, a 2-MHz system clock, and CPU support hardware and logic for i/o to user control interfaces and peripheral devices.

Memory mapped and bused i/o structure permits the Z80's memory reference instructions to be used when i/o operations are executed. The board is suited for use in dedicated industrial microcomputer control systems, for applications requiring large program or fixed data memories, and for those requiring special i/o equipment and multiplexing/demultiplexing of many i/o signals.

Additional features include automatic power-on restart, jumper selectable serial i/o data rates, interrupt capability, and DMA. Program devel-

opment in both assembly language and FORTRAN is supported by the company's line of MM1 microcomputer development systems. Compatible microcomputer plug-in boards including memories and i/o interfaces are also available.

Circle 176 on Inquiry Card

FORTRAN Compiler Operates on Minifloppy/ Microcomputer System

A FORTRAN compiler, operated by the company's system 8 (see *Computer Design*, June 1977, p 220) under the CP/M disc operating system, features all ANSI standard FORTRAN, X3.9-1966. FORTRAN functions are implemented with 32-bit floating point arithmetic; integers are implemented with 16-bit numbers. Compiler and subroutine library produce compact object code.

Gnat Computers, Inc, 7895 Convoct Ct, Unit 6, San Diego, CA 92111 later will be adding double precision and complex numbers to the compiler. A relocating assembler, linking loader, and FORTRAN library are also included.

Circle 177 on Inquiry Card

BEEHIVE INTERNATIONAL'S B500 IS FLEXIBLE



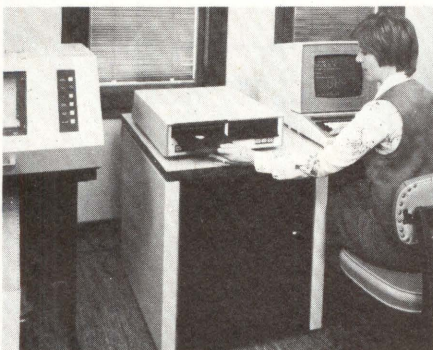
1. Our B500 is an 8080A micro-processor based video display terminal



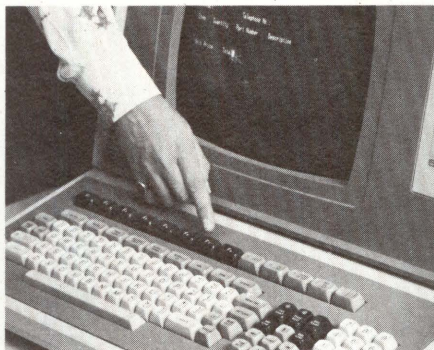
2. It is user programmable
*Controller Panel
Programming Manual*



3. It has an expandable memory
*Display-4K RAM (4000 Characters)
Program-Up to 4K PROM or 7K ROM
-Up to 48K RAM*



4. Beehive's B500 provides a printer port for printing requirements and an auxiliary port to accommodate floppy disks



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Microcomputer System Offers Fast Access With Minifloppy Discs

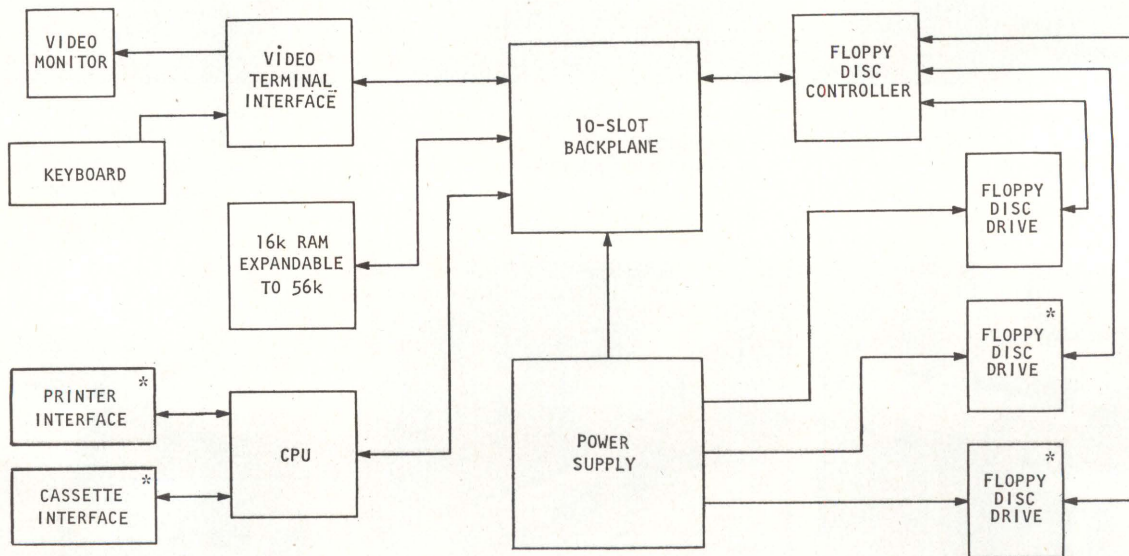
Disc-based microcomputer system 8813, capable of performing interactive computing applications, consists of a rack mountable chassis, power supply, walnut cover, fan, and

10-slot backplane. Installed in this backplane are an 8080A CPU/ROM/RAM card, video terminal interface card, 16k bytes of read/write memory, and floppy disc controller card. One floppy disc drive is included, with room for a total of three.

PolyMorphic Systems, 460 Ward Dr, Santa Barbara, CA 93111 has

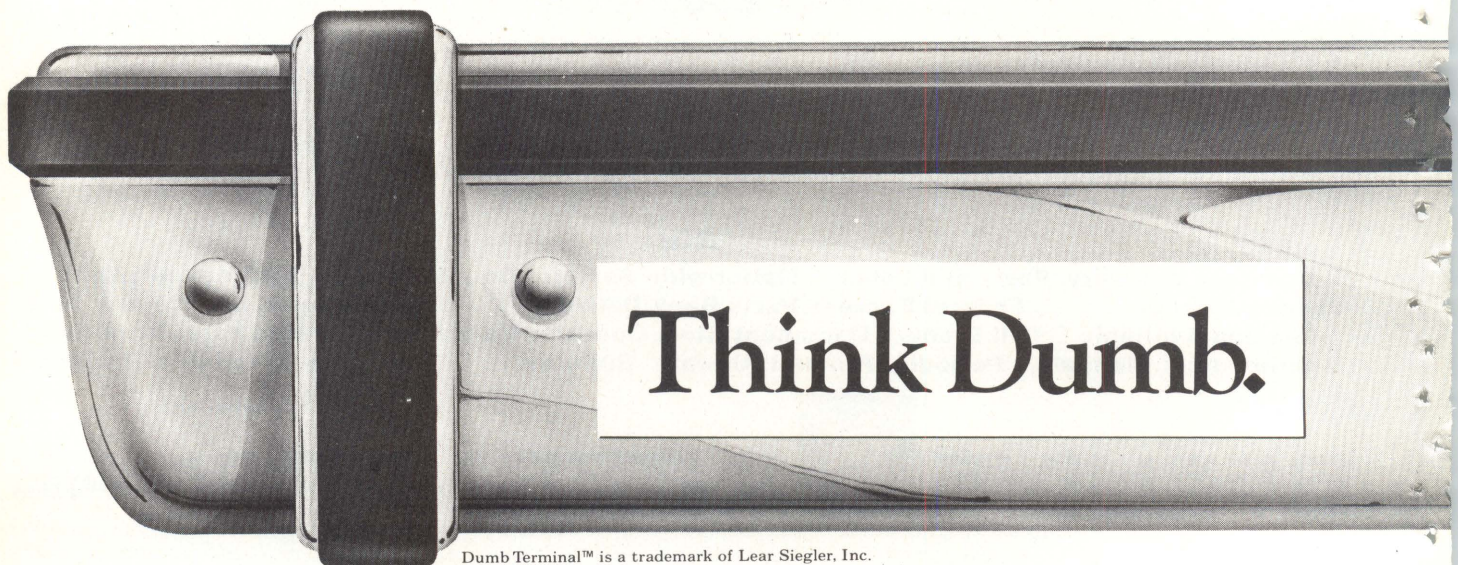
also included a graphics/alphanumeric video monitor, detachable keyboard with cable, and system software on diskette with the package. Either assembly language or fully extended 11k BASIC can be used to run applications.

Use of discs enables storage and fast access to programs and data. An executive program handles communication between the user and the rest of the system. In addition to this level, the system also may operate at the subsystem level.



*OPTIONAL

Disc-based microcomputer system from PolyMorphic Systems includes CPU with 3k p/ROM, system RAM, two serial I/O ports, vectored interrupt, and real-time clock. Software comprises complete disc operating system, BASIC, video-based editor, assembler, and debugging aids



Dumb Terminal™ is a trademark of Lear Siegler, Inc.

Component Provides Low Cost Microprocessor Power Source

Availability of the model 3M5U12-5 dc-dc power source developed for MPUS, RAMS, EROMS, and other microprocessor-related ics has been announced by Reliability, Inc, 5325 Glenmont, Houston, TX 77036. The device provides 12 V at 300 mA and -5 V at 100 mA from a 5-Vdc input; outputs are fully short-circuit protected and free from overshoots.

Features include an operating temperature range of -25 to 70°C still air and 300-V input to output isolation. An efficient input filter incorporated in the 2 x 2 x 0.4" (5 x 5 x 1.01-cm) units limits the input reflected ripple to 5 mV rms. All of the devices are burned in and triple tested.

Circle 178 on Inquiry Card

Increased Capabilities Obtained With Single and Triple Processor Systems

Designed around the model 500 CPU board, the Challenger II computer is equipped with 256k-byte memory management and 8k BASIC in ROM option. It can be operated at either 1 or 2 MHz. Additional features include 4k RAM on the CPU, serial port on CPU, and software compatibility with the original model.

Ohio Scientific, 11681 Hayden, Hiram, OH 44234 is offering the system in video form (as the IIV) and in a 4-slot version with captive keyboard (as the IIP). Complete

with BASIC in ROM and RAM (4k), the IIP is a self-contained personal computer with full-size keyboard and 32 x 64-character video display interface. Containing an audio cassette interface, the system connects to a monitor or TV set via an RF connector (not supplied) and optionally to a cassette recorder for program storage.

A triple processor CPU board is contained in the Challenger III which runs 6800, 6502, 8080, and Z80 programs. The OS-65D disc operating system is standard. In addition to educational, small business, and personal applications which are served by the other models, the III also meets industrial development needs. A software processor status switch for writing multiple processor programs is optional. Support for all systems includes software library, mainframe expandability, and existing accessory line.

Circle 179 on Inquiry Card

Single-Chip μ Computers Are Effective in Control, Computation Situations

One solution to the application of microcomputer technology to high production volume industrial and consumer products is a broad family of cost-effective single-chip microcomputers. The μ COM 4 family of 4-bit LSI microcomputers is currently comprised of four members; additional members with extended capabilities are to be introduced in early 1978.

Similarities among the microcomputers include an ALU, user-specified

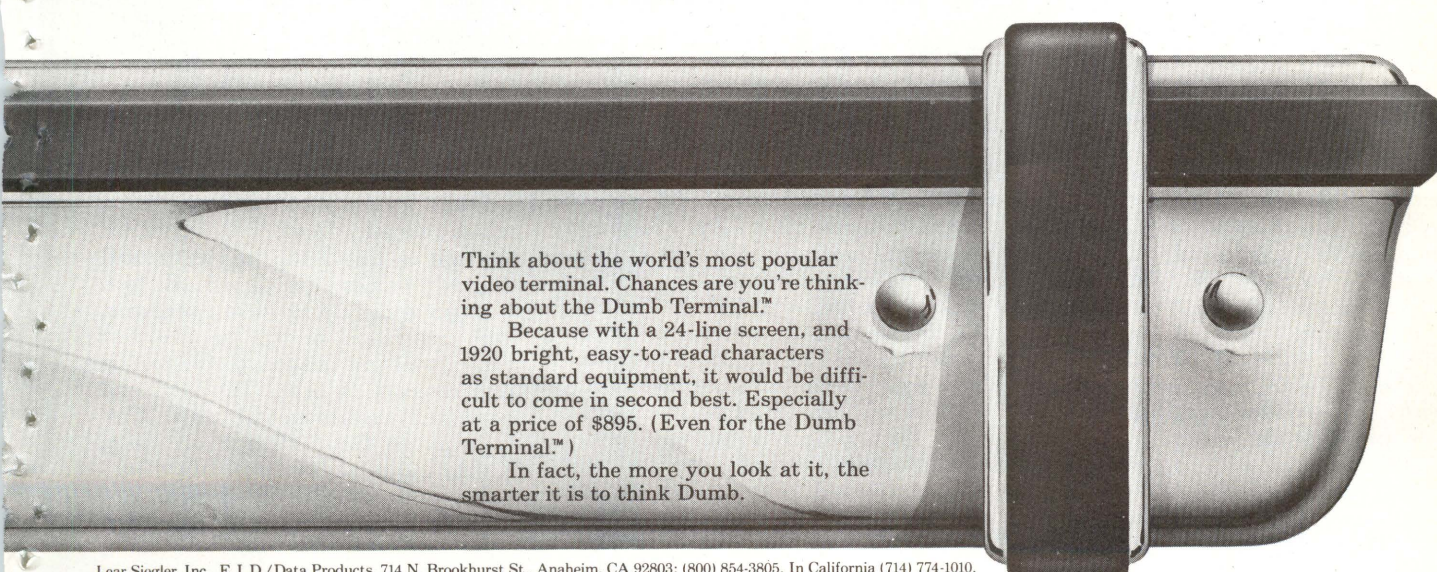
masked ROM for program storage, RAM for data storage, and multiple i/o lines. A powerful applications-oriented instruction set featuring multifunction instructions is common to all. NEC Microcomputers, Inc, 5 Militia Dr, Lexington, MA 02173 offers full documentation, prototyping tools, software, and software development systems as support.

Each is a p-mos processor packaged in a 0.6" (1.5-cm) wide plastic DIP, requiring only a 10-V power supply. μ COM-42 has 1920 x 10 bits of ROM, 96 x 4 bits of RAM, 35 i/o lines, and 72 instructions; -43 has a 2k x 8-bit ROM, 96 x 4-bit RAM, 35 i/o lines, and 80 instructions; -44 has a 1k x 8-bit ROM, 64 x 4-bit RAM, 35 i/o lines, and 58 instructions; and the -45 has 640 x 8 bits of ROM, 32 x 4 bits of RAM, 21 i/o lines, and 58 instructions.

SC/MP CPU Card Is Self-Contained With Onboard Memory

PDC-100, bus- and card-size compatible with the National ISP and the company's PDC card family, features a SC/MP II CPU chip, 256 bytes of RAM, and up to 1024 bytes of bipolar p/ROM. MilerTronics, Div of George Miler, Inc, 303 Airport Rd, Greenville, SC 29607 offers the card with onboard RAM and p/ROM; it can run without supporting logic or cards and can control memory and i/o cards in bus-type systems. Added features include 600 ns/microcycle, single 5-V supply requirement, and 15-card fanout.

Circle 180 on Inquiry Card



Think about the world's most popular video terminal. Chances are you're thinking about the Dumb Terminal.™

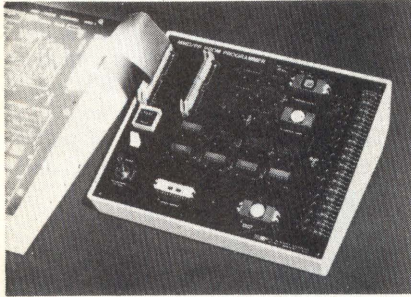
Because with a 24-line screen, and 1920 bright, easy-to-read characters as standard equipment, it would be difficult to come in second best. Especially at a price of \$895. (Even for the Dumb Terminal.™)

In fact, the more you look at it, the smarter it is to think Dumb.

Lear Siegler, Inc., E. I. D./Data Products, 714 N. Brookhurst St., Anaheim, CA 92803; (800) 854-3805. In California (714) 774-1010.

Time Saving, Low Cost Accessory Programs EPROMs

The 1702A EPROM programmer (MMD-PP) for the Mini-Micro Designer training and development microcomputer can program a 2048-



bit EPROM in approximately four minutes by sharing the microcomputer circuitry under control of a special p/ROM. The EPROM accepts data from any memory block or from any p/ROM designated as a master. After programming, the contents of the EPROM can be verified against those of the memory source or master p/ROM.

Data transfer between the microcomputer and programmer introduced by E&L Instruments, Inc, 61 First St, Derby, CT 06418 takes place over a 40-pin connector and ribbon cable assembly. The self-contained power supply operates from a 115-/230-V, 50- to 60-Hz line.

Circle 181 on Inquiry Card

Video Display, I/O, and Analog Boards Enlarge Microcomputer Family

The MCB family of Z80-based microcomputer boards has been expanded by Zilog, Inc, 10460 Bubb Rd, Cupertino, CA 95014. Containing 256 bytes of RAM, the Z80-VDB video board interfaces the Z80-MCB directly to TTL horizontal, vertical, and video drives of a standard tv monitor.

The Z80-IOB input/output board with four parallel interface controllers provides the company's microcomputer users with programmable control of up to 64 i/o lines. The eight serial (four full-duplex) channels of the Z80-SIB serial i/o board are each capable of synchronous or

asynchronous data transmission including Bi-Sync protocol.

For process control and instrumentation uses there are two analog boards. The Z80-AIB input board has 32 single-ended input channels, ADC gain ranges of 0 to 5 V up to 0 to 10 V, and amplifier gain ranges of 0 to 1000. The Z80-AIO input/output board has 32 analog channels in and two analog channels out. Output voltage ranges include 0 to 10 V, ± 5 V; and 0 to 5 V, ± 2.5 V at 5 mA.

Circle 182 on Inquiry Card

Microcomputer and Peripheral Second Sourced

Fairchild Camera and Instrument Corp, 464 Ellis St, Mountain View, CA 94042 and Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006 have concluded an agreement which enables Fairchild to second source the Mostek 3870 microcomputer and 3871 peripheral input/output circuit. Fairchild will receive mask sets, technical data, and documentation relating to the two devices.

The 3870 is a single-chip, 5-V, n-channel microcomputer with 64 bytes of RAM, 2048 bytes of ROM, 32 bidirectional i/o ports, and a time event counter. Fully compatible with the F8 microprocessor family and capable of using the same hardware and software design aids, the device expands Fairchild's microprocessor capability.

Circle 183 on Inquiry Card

Software Products Are Supplements to Microcomputer System

Four enhancements to the MDS-800 equipped with either the Z80 system adapter module or Z80 in-circuit emulator are available from Relational Memory Systems, Inc, PO Box 6719, San Jose, CA 95150. The Z80 macro-relocatable assembler implements the full set of Z80 mnemonics and generates relocatable code compatible with the Intel MDS-800 link and load programs running under ISIS-II; other versions operate with ISIS and standalone versions of the MDS. Relocatable modules written in PL/M 8080 or 8085 assembly language can be combined and linked

together with those written in Z80 assembly language.

The source translator utility converts 8080 or 8085 assembly language source programs to Z80 assembly language. The 8080 programs are translated and optimized with Z80 instructions resulting in improved program execution speed and reduced memory requirements.

A fast diskette copy and compare utility operates with ISIS or ISIS II, performing an exact copy of any diskette mounted in drive 0. Execution time is 2.5 min. Not limited to ISIS system discs, the utility checks for both hardware and data errors.

Running under ISIS or ISIS II, the universal load utility loads (and optionally compares) a user specified hex file directly into MDS RAM, or stores a specified RAM area as an ISIS file. Dump/restore capability is for checkpointing programs under modification, and as a general-purpose memory to disc/disc to memory utility.

Circle 184 on Inquiry Card

Device Offers Accurate Environmental Simulation Test Programming

Providing digital accuracy, the Key Command I, model 013024/25 microcomputer programmer features a



lighted annunciator display panel which visually leads the operator through a test setup sequence and displays values during actual test. Unit programs up to 50 test segments with repetition of up to 200 test cycles, meeting mission profile testing requirements of MIL-STD-781C and combined environmental tests. Unit is available from Thermotron Corp, Kollen Park Dr, Holland, MI 49423 either separately or in System 211 with temperature controller, recorder, and Productsaver temperature limit.

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Anode lead wire for impressed current anodes for use in deep ground beds, sea water and other severe cathodic protection environments.

Jackets for use as cladding over glass fiber bundles in transportation applications utilizing fiber optics.

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Solder Sleeves® provide electrical solder connections for wires, cables, cable shields and coaxial cables.

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KYNAR® Resin protects your wiring system end to end.

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Kynar can be marked, printed, striped, or hot stamped for identification. It can also be pigmented for color coding.

Kynar has high dielectric strength and good insulation resistance.

Kynar has a temperature range from -80° to $+300^{\circ}$ F.

Kynar is nondripping, self-extinguishing (UL STD 94 V-0) and has an LOI (Limiting Oxygen Index) of 45.

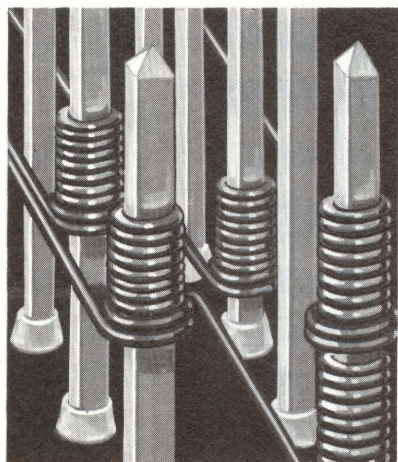
Kynar has good chemical resistance, low permeability.

Kynar has a tensile strength of 7000 psi. It is mechanically strong and has good abrasion and cut-through resistance.

Kynar has low-moisture absorption (0.04%), excellent radiation and UV resistance.

For list of fabricators, more technical data, specifications (UL and military), write or call Joe Michaud, Plastics Department, Pennwalt Corporation, Three Parkway, Philadelphia, PA 19102. (215) 587-7520.

*KYNAR is Pennwalt's registered trademark for its polyvinylidene fluoride resin.
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Kynar insulated wire is ideal for automatic wire wrapping operations for computer back panels.

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Have The LSI Parts You Buy Been Thoroughly Tested?

Eric R. Garen

Integrated Computer Systems, Inc
Culver City, Calif

When a designer incorporates LSI chips into his system it is essential that he know that they have been tested. Usually he can assume that they were, but the question then becomes: how thoroughly? The answer to this will impact both reliability expectations and vendor selection.

Prime objective of the semiconductor manufacturer when testing is to reject the largest number of bad parts without incorrectly rejecting good ones. Tests, however, must be nondestructive so as to minimize loss of product due to improper application. Finally, they must be quick and inexpensive.

Obviously there are conflicts among these objectives. The manufacturer is motivated to minimize testing costs while assuring a high enough quality level to prevent loss of customers. Since testing costs are typically in the neighborhood of \$0.20 to \$0.40 for LSI parts, they have a major impact on profitability of high volume parts in the \$2 to \$4 price range.

Tests are performed at several points during the device fabrication process (Fig 1). First, a wafer test checks that each wafer was processed according to the requisite control parameters, such as gate threshold, metal field threshold, and polysheet resistance. Next, the wafer sort procedure separates good and bad dice by testing at room temperature to determine which dice perform the basic device function. Dice that fail this procedure are often subjected to diagnostic testing to obtain information for process engineers to use in improving yields; dice which pass are packaged and sometimes burned-in for a 1- or 2-day period.

Every part is then subjected to a final test, typically performed at elevated temperatures to classify the components into different grades of performance and operating margins. As a last procedure, QA tests are performed on statistical samples selected from each lot to catch errors due to incorrect sorting of good and bad parts, and to find parts that were subjected to incorrect test procedures, were tested by systems out of calibration, or might have been destroyed by improper handling after performance of the final tests.

Tests used in wafer sort and final test are the result of a continuous development program. Initially, test programs for new parts are specified by the designer of the part and rely heavily on his knowledge of the sensitivity of the circuit to parameter variations. By analysis and experimentation on different lots, these tests are honed; however, the initial testing of new products is typically extremely long and may include tests that later turn out

to be unnecessary, for example, tests used to qualify the design and process. These tests gather data for establishing worst case timing and voltage conditions or worst case pattern to be used in later versions of the program.

A typical test program includes continuity test, shorts and open test, gross functional test to determine operability under normal conditions, high voltage stress test which attempts to accelerate failures due to latent defects, leakage test, and detailed functional tests of the device under various combinations of power supply, temperature, and input/output timing to determine proper operation under expected worst case conditions. For example, a typical test for a 4k dynamic RAM might include

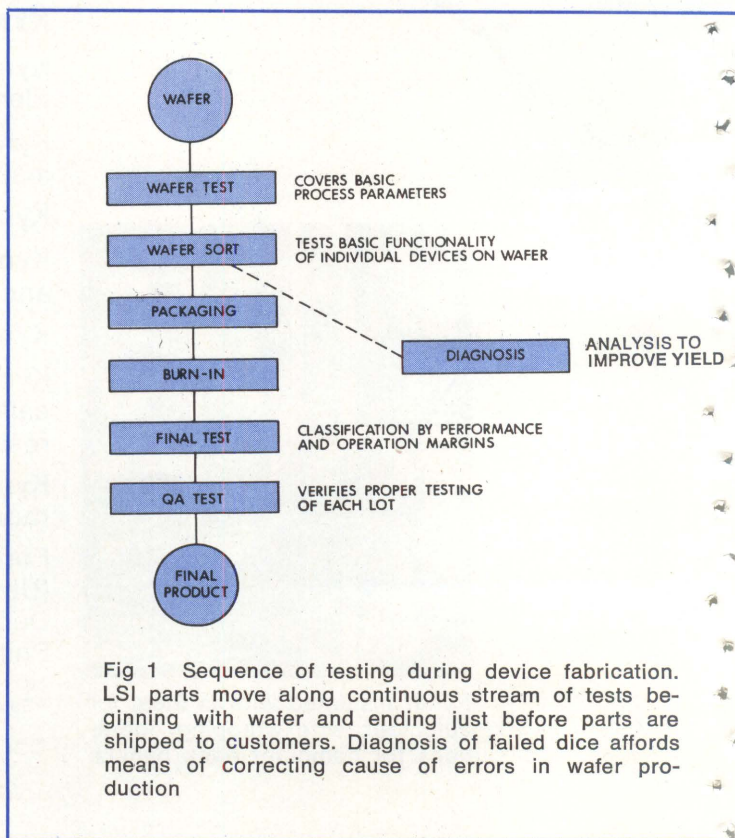


Fig 1 Sequence of testing during device fabrication. LSI parts move along continuous stream of tests beginning with wafer and ending just before parts are shipped to customers. Diagnosis of failed dice affords means of correcting cause of errors in wafer production

a series of simple pattern tests (such as checkerboard and diagonal patterns) performed at the four worst-case combinations of V_{DD} and V_{BB} (drain and base supply voltages, respectively). More comprehensive patterns, such as walking columns, may also be tested at these four extremes or may be tested at just the very worst two cases (V_{DD} min/ V_{BB} min and V_{DD} max/ V_{BB} max). These tests are intended to insure that the RAM functions with worst-case timing specifications over the full power supply range.

Despite these tests, faults will remain undetected. For example, testing at the four voltage extremes does not necessarily guarantee proper response to all possible voltage combinations. More comprehensive tests varying both voltages continuously over the full range may locate failures not found by worst-case testing. These test results are usually presented in a "shmoo plot" which indicates circuit response (either detailed timing response or pass/fail response) versus variable parameters such as supply voltages and input signal timing.

Many testing services claim that "4-corner" testing is inadequate for complex LSI devices. A case supporting this claim is shown in Fig 2. Note that while the devices passed the tests at the worst-case combinations of parameters, they failed at intermediate points.

How often are device failures detected after delivery? Testing labs with experience in high volume testing of 4k dynamic RAMs indicate that results can vary widely from one semiconductor manufacturer to another. The lowest attrition rates are typically 1 to 1.5% for comprehensive go/no-go testing after burn-in. However, thorough testing sometimes rejects more than 50% of some lots from certain inconsistent manufacturers. Similar results have been found (although based on lower quantities) on microprocessors and other dynamic LSI circuits.

Some of these faults result from semiconductor manufacturers changing die design or shrinking die size to reduce costs and/or improve yields. Although nominally the

same part number is being bought, it may be faster than expected and cause race conditions or some other unexpected result. Another reason is that LSI manufacturers can not predict the user's system interaction problems and therefore cannot completely test the LSI device.

Based on these results, it is worthwhile for a designer to perform his own LSI component burn-in and test prior to PC board production. This is especially important to minimize rework and warranty costs for systems using more than 20 LSI parts. With 20 parts, even the best reject rate of 1.5% results in only a 74% probability of system success. If a "bad" lot results in only 5% failures, the system stands less than a 36% chance of functioning properly.

As a practical example, consider the case of memory board testing where more than one memory IC in an array fails. This could cause a row and column to fail; to find the bad part requires progressively removing components in a pseudobinary search mode or cutting PC lines which must be later repaired. If presolder testing can get failures down to one component in an array, it can usually be isolated directly. Consider, too, warranty costs; one field repair trip at \$25/h labor, with overhead, and with related system downtime greatly overshadows all additional component, board, and system testing done during manufacture.

Thus, testing is certainly desirable. However, most users do not have production volumes to warrant the purchase of LSI test equipment (\$30,000 to \$300,000). In that case, the services provided by testing laboratories may be cost-effective despite the relatively high cost (5 to 30 cents per part and another 20 cents for burn-in). These costs might well be saved many times over in reduced rework and field repair.

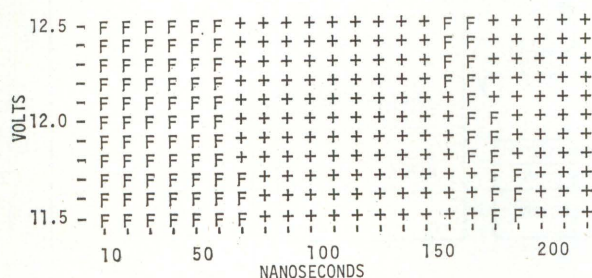
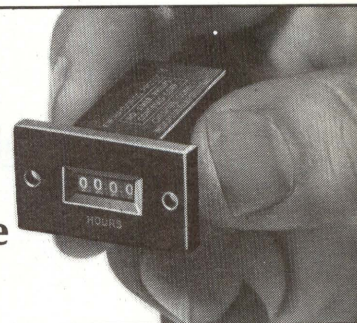


Fig 2 Shmoo plot shows failures occurring at various combinations of V_{DD} and address hold times other than extremes of these two parameters. Testing only extremes runs risk of passing parts that will fail at other combinations of those two parameters

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For information only, circle 88 on Inquiry Card.

Dual Addressing DMA Controller Serves as Special-Purpose Processor

A repertoire of six command bytes, each specifying a number of functions, are contained in the Z80™-DMA programmable, single-channel DMA controller. The device provides all address, timing, and control signals needed to perform memory-to-port, port-to-memory, memory-to-memory, and port-to-port data block transfers at data rates up to 1.25 MHz. Moreover, the device is able to program data transfer timing to match any port speed. Beyond transferring data, however, the controller performs memory search as well as search-and-transfer operations and can interrupt on four conditions: ready, search-match, end-of-block, and search-match at end-of-block. In addition, all data transfer under any one of four programmable bus disciplines: cycle-stealing, byte-at-a-time, burst, or continuous.

To facilitate data transfers, the device contains two 16-bit address

registers, a block length register, and counters associated with each, thus providing address buffering (block diagram). During a transfer, data are read from one port and written to another, with associated counters being incremented, decremented, or held constant under program control until completion; whereupon, the transfer ceases.

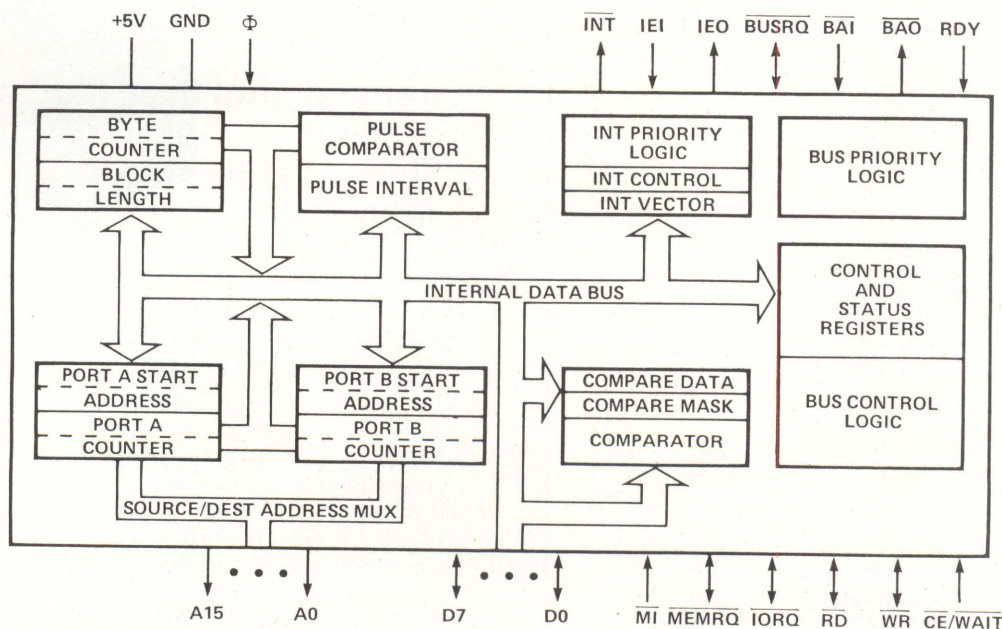
During search, data are only read and those bits not masked by the mask register are compared with the compare register contents. A match halts the search. In a search-and-transfer operation, data move until a match is found or end-of-block is reached, after which the operation stops. At the completion of any of the three operations, an interrupt may be generated.

Another feature available during a transfer is the ability to load the pulse interval register with a byte count which is compared with the

byte counter contents as each byte transfers. When a match occurs, a signal is sent to the peripheral controller receiving the data. This is useful, for example, in delimiting sectors during transfer to a disc controller.

Completion of a transfer and/or search is relayed to the CPU via controller interrupts. The nature of an interrupt condition is detailed by one of four interrupt vectors which originate from the interrupt vector register. This register can contain a base vector corresponding to the ready interrupt condition that can be altered to produce three more vectors representing end-of-block, search-match, and search-match at end-of-block.

End-of-block and search-match vectors signal completion of transfer and/or search operations, while the search-match at end-of-block vector indicates the special condition of a match found at the end of a block



Z80-DMA internal block diagram. Shown are dual addressing feature, register buffering capability, byte counter that permits block transfers, comparison logic which enables search operations, interrupt logic that produces four interrupt vectors, and bus control logic that effects any one of four bus disciplines

How FORTH™ software tools have rescued mini and micro project developers reads like a fairy tale.



A short time ago, a gloomy Monday found a New York manufacturer desperate. Microprocessor software problems had deep-sixed the delivery date of an artificial-kidney tester.

Four man-months of assembly language programming...and still the device wouldn't work.

Came Tuesday, design specs were rushed to a group of software problem-solvers, FORTH, Inc. Three nights a crack FORTH programmer concentrated on saving the day...flying cross-country to project headquarters on Friday.

By Sunday night, the machine was totally operational!

Five FORTH days, with one man applying microFORTH language and programming techniques, and the tough software task was fully written, debugged and cross-compiled.

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The hang-up? High level languages demanded too much memory; but assembler code, too much development time.

Fortunately, project management was wise to FORTH's track record in image processing. And the availability of off-the-shelf miniFORTH software that could accommodate just about any-make mini...on order, on hand, or on line.

National secrets can't be spilled, but what can be told is the performance of miniFORTH tools in the hands of *typical* users: software development time, 3-10 times less. Memory requirements reduced up to 50% over assembly code, with full machine speed capability. All simultaneously!

Easy to see why the Navy selected FORTH as the sole source for this software contract.

Software development time:
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FORTH
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FORTH is fact...not fable. There is a popular myth: it says you can optimize today's advanced mini/micro hardware — with software tools as old as some programmers. But wishing won't make it so; you need rich new programming techniques.

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microFORTH runs on disk-based micro-processor development systems, package-priced at \$2500, plus options.

So flexible, so powerful are FORTH capabilities, our case histories strain credulity. We admit it. And we admit, to learn this new shortcut, you'll leave the old-shoe comfort of Basic and Fortran behind.

It's worth it. In cost-effectiveness. In dramatic cuts in development time. In much lower computing-equipment investments. Just what it takes to make heroes in real life.



Moral. You don't have to believe in fairy tales, to know that the limitations of Basic, PL/M, and Fortran are often pretty grim. Calling FORTH in late can save your neck. But calling FORTH *first* can make any software project easier to swallow.

Phone (213) 372-8493, for microFORTH, miniFORTH or programming assistance. Or write: FORTH Inc., 815 Manhattan Avenue, Manhattan Beach, CA 90266. We can help.

FORTH, Inc.

CIRCLE 89 ON INQUIRY CARD

being transferred. The base vector generates an interrupt each time the controller is about to access the bus. This affords the CPU the ability to restrict the controller's access to the bus when necessary.

When the controller does access the bus, its ability to specify cycle-stealing, byte-at-a-time, burst, or continuous bus access permits it to serve the CPU and system peripherals more efficiently. Using cycle-stealing in buffered systems, the device steals memory refresh cycles from the CPU to effect its transfer without degrading program execution speed. For faster transfers or where refresh may not be interrupted, the byte-at-a-time method allows the controller to access the bus for a single byte transfer after which control returns to the CPU. The process repeats for each byte transferred so that the CPU and the device interleave their cycles.

For high speed operation, burst and continuous access to the bus provide the fastest data transfer. The two differ only in their reactions to an idle condition at the port being serviced. Burst access relinquishes control of the bus if the port being serviced goes idle, while continuous access relinquishes control to the CPU only after the entire data block specified has been transferred.

One other way the controller optimizes system interaction is by ad-

justing its transfer rate under program control to exactly match that of the system memory and peripherals. This, moreover, eliminates the need for external signal conditioning logic. Timing can be reduced from the maximum 1.25-MHz rate in four increments. Thereafter, using one of the steps in concert with the controller's $\overline{CE}/\overline{WAIT}$ input line, which idles the device when active, any port speed can be matched.

Capabilities of the controller, which is manufactured by Zilog Inc, 10460 Burbank Rd, Cupertino, CA 95014, are controlled by six command bytes and associated read, interrupt control, timing control, and status bytes. Command structure of the device is such that bits of one command alert the controller to expect a particular byte to follow and detail where the byte is to be moved within the device. Receiving a sequence of commands and associated bytes from the CPU in advance of a transfer and/or search operation, the controller configures its capability to perform the requested operation and thereafter carries out the operation.

The device operates from a 5-V $\pm 5\%$ supply over the 0 to 70°C temperature range. Packaged in a 40-pin plastic or ceramic DIP, it is expected to sell at a price close to that of the Z80A CPU.

Circle 350 on Inquiry Card

put drive application, results in much wasted power; whereas, tailoring the base drive specifically for the 100-mA application results in considerable power savings.

Another benefit resulting from this bias arrangement is a relatively low saturation voltage for a given drive current. A 300-mA sink current in a driver connected to a 48- Ω load and externally biased with a 650- Ω resistor results in a typical 420-mV saturation voltage. Without the base drive, saturation voltage in excess of 1 V would be required.

Manufactured by Texas Instruments Inc, PO Box 5012, Dallas, TX 75222, each driver offers a 40-ns low-to-high and 30-ns high-to-low typical propagation delay while responding with a 20-ns low-to-high and 15-ns high-to-low typical transition time. Characterized to operate from 0 to 70°C, the SN75328 is housed in a 16-pin plastic or ceramic DIP while the SN75330 is only available in a 20-pin plastic DIP.

Circle 351 on Inquiry Card

Bipolar p/ROM Contains Built-In Power Switching Circuit

Power switching, a technique for reducing overall power dissipation of large p/ROM arrays by switching off the supply voltage (V_{cc}) to all unselected p/ROM devices, has now been extended to a switched p/ROM (SPROM) which contains built-in power switching circuitry. An open-collector version of the device affords a 90% power savings while a 3-state version provides 75%. This results in a typical 100- to 150-mW power dissipation, open-collector and 3-state, respectively, when power is switched. As an example, a 1024-word x 16-bit/word memory constructed with conventional 256 x 4 p/ROM consumes approximately 8 W; using SPROM and switching three of the four banks off while the fourth is read results in a 75% power savings, or roughly 6 W.

Power SPROMs offer the designer full V_{cc} tolerances of 5% for a commercial version and 10% for a military, and guarantee address access time of typically 35 ns and enable access time of typically 40 ns. Design compromises to achieve power reduction in external switching circuitry are therefore eliminated.

Memory Switches Interface Both Core And Bubble Memories

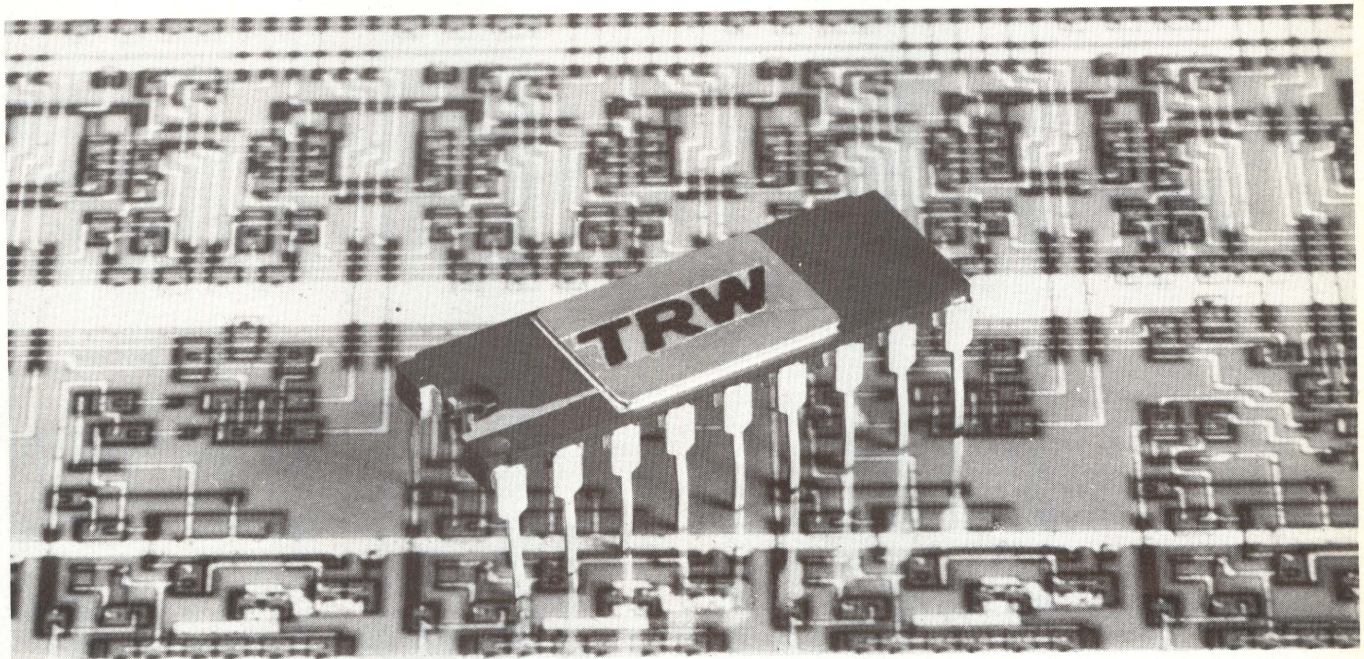
Quadruple memory drivers—monolithic IC memory switches with TTL inputs—serve as interfaces to both core and bubble memories. Each of the four drivers in the type SN75328, SN75330 memory switches is capable of driving a 600-mA load while requiring only a minimal 600-mV saturation voltage at typical 40-ns switching speed. The quad drivers' dual capability results from the ability of the voltage at the driver output transistor to swing between the supply voltage (V_{cc}) and ground.

Comprising an npn transistor which provides sink drive when its emitter is tied to ground and collector to a load, and source drive when its emitter is tied to a load and collector to V_{cc} , each driver receives a 5.5-V, TTL- or DTL-compatible enable input via a diode-clamped Darlington driv-

er connected to the transistor base. Diode-clamping in the Darlington driver ensures that a negative-going input does not damage the driver transistor, while similar diode-clamping at the driver output affords transient voltage, inductive kickback, protection from the load.

Variable drive current with resulting lower overall power dissipation is achieved by externally biasing the Darlington base driver which, in turn, regulates the driver transistor. This is accomplished by connecting an external resistor between V_{cc} and the IC's node R input. In the SN75328 a single node R input results in all drivers receiving the same base drive; while in the SN75330 an individual node R input per driver allows individual base drive levels. To demonstrate the value of this, a 100-mA output drive application which requires only a 10-mA base drive, receiving the 50-mA base drive typically required for a 500-mA out-

8-Bit high-speed monolithic A/D



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TDC-1002J	1000 ns	\$75 in 100's
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Two performance ranges—400 and 1000 ns conversion times: two price ranges for a wide variety of high-speed A/D applications.

Linearity is $\pm 1/2$ of LSB. Nine clock periods per conversion. All output bits are ready one clock period after the status signal indicates "ready to convert." There are no missing codes — ever!

TDC-1001J and TDC-1002J are supplied in an 18-pin ceramic DIP package designed to operate at a commercial temperature range of 0° to 70° C.

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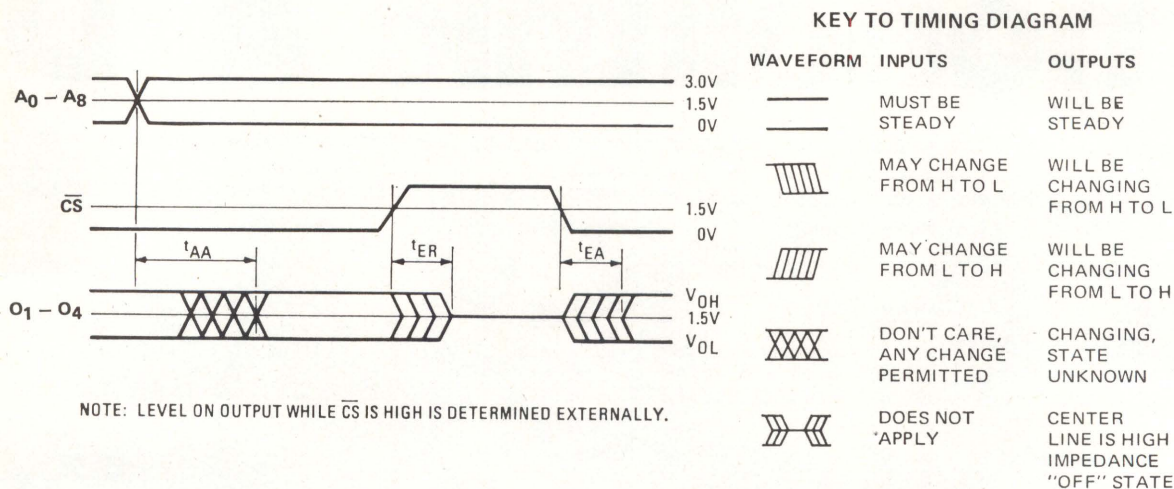
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CIRCLE 90 ON INQUIRY CARD



Switching waveforms for 512 x 4 SPROM. Timing shows typical 35-ns address access (t_{AA}), 40-ns enable access (t_{EA}), and 15-ns enable recovery (t_{ER}) times. Actual memory access time, if chip-select (\overline{CS}) lines as is usually done, is the 40-ns enable access time

Manufactured by Raytheon Co, Semiconductor Div, 350 Ellis St, Mountain View, CA 94042, the 512 x 4 and 256 x 4 field programmable memories contain address-select lines (nine on the 512, eight on the 256), four output pins, and a chip-select (\overline{CS}) input which activates the power switch in the memory (waveform diagram). Address and \overline{CS} levels are typically presented to the respective inputs simultaneously. The resulting output drive from each output data line is typically 16 mA.

All inputs and outputs are TTL-compatible. Storage elements are nichrome fusible links manufactured with each element in a high output state. Programming the memory involves blowing individual fusible links to produce a low output.

To select a particular link for programming, the word address is presented at TTL levels to the address-select (A_0-A_8 on diagram) with a V_{CC} of 5.50 V applied to the chip. Then both the \overline{CS} input and the individual output pin (O_1-O_4) being programmed are pulsed with a higher amplitude pulse than normal to supply the required current to program the link. Only one output pin can be programmed at a time, because internal decoding circuitry is capable of sinking only one bit at a time.

To ensure that the output transistor containing the link to be pro-

grammed is off before pulsing the output pin, the pulse to the \overline{CS} input must occur at least 100 ns before the output pin pulse. Since the fusible link blows on the rise time of the pulse, both the \overline{CS} input and output pin pulse must have a 50 ns to 70 ns rise time. After programming the link, it can be checked for a low by enabling the \overline{CS} input and observing a low at the output pin.

Operating temperature range for the commercial grade chip is 0 to 70°C while the military grade operates over the -55 to 125°C range. All parts are available in 16-pin DIPs.

Circle 352 on Inquiry Card

Reduced Standby Power Improves Economy of High Density RAM Systems

Combining HMOS (high performance mos) technology and a newly developed low power standby mode, the 2147 and 2147-3 4k static RAMs consume 500 and 600 mW of power, respectively, when selected, but use only 50 and 70 mW when in standby (ie, not selected). The RAM family's 45-ns typical cycle time, which is its access time as well since the memory is static, results from the HMOS tech-

nology that incorporates onchip substrate bias generation in combination with device scaling.

Most power consumption on conventional static memory results from supplying constant current not only to the flip-flops containing the stored data bits on the chip but to the peripheral circuits about each flip-flop as well. In standby mode, power to these peripheral elements is turned off, leaving only a minimum current to power the storage flip-flops and thus providing the power saving feature. Power to drive the peripheral circuits during memory access is activated with the RAM's chip-select (\overline{CS}) input (diagram). Since this input is not a clock and need not be cycled, it can be tied directly to system addresses and used as part of normal decoding logic. Moreover, when the input falls, power to the RAM reverts to the standby level, without need to lower power supply voltage to the memory.

This reduced power operation offers significant advantage to large memory systems as well as to systems operating with an imposed system cycle longer than the memory access time. In memory systems larger than 4k which continuously access memory (100% duty cycle), only one 4k memory block is active at a time; thus total system power requirements fall asymptotically toward the stand-

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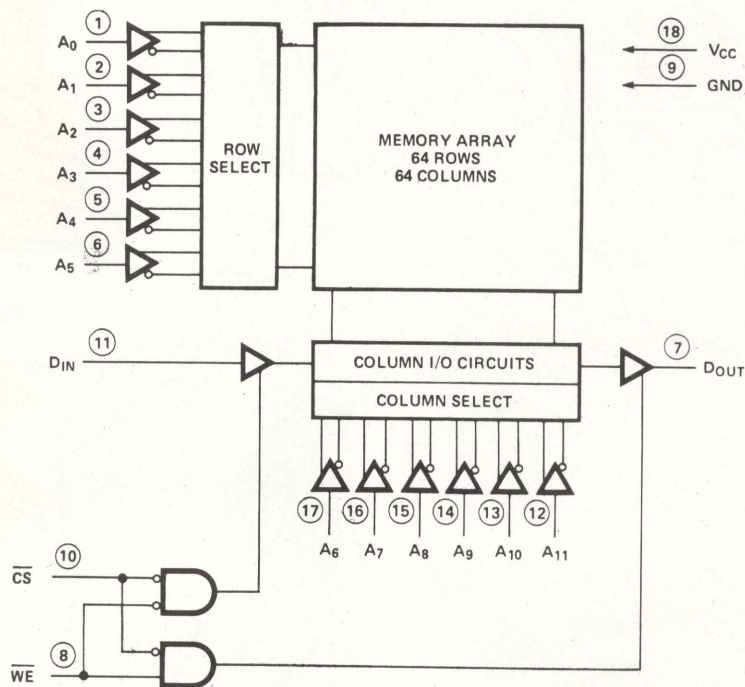
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Block diagram of Intel 2147 4k static RAM. Automatic power-down feature for standby mode is controlled by chip select (CS) input. In this mode, power to peripheral circuits about unselected flip-flops is turned off

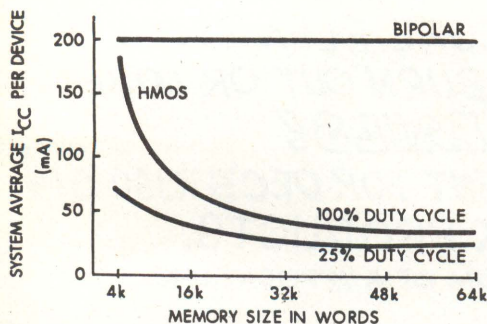


Chart of power requirements vs system size for high performance MOS devices compared to bipolar. With continuous memory access (100% duty cycle), power consumption falls asymptotically as memory size increases since at any time only one 4k increment is drawing high active current while all others draw lower standby current. The same is true for a 25% duty cycle, with a further power savings due to all of memory being inactive 75% of each system cycle

by power level as memory capacity increases. This results in power savings as great as 85% in larger systems. Moreover, in systems with a cycle time greater than memory access time, eg, 25% duty cycle, still larger power savings result as memory capacity rises since all memory is inactive for a portion of the system cycle time. The reduced power advantage also appears in reduced cooling and power control problems which typically grow linearly with increasing storage capacity when using conventional static memory.

Since they are static or unlocked devices, the RAMs do not require address setup and hold timings; thus the chips can be selected before, during, and after an address change. Moreover, inputs and output are unlatched. Besides the chip-select input, which cues a RAM's active and standby modes, a chip contains 12 address-select lines, a write-enable input, a data input, and a separate 3-state data output, all of which are TTL-compatible. Capable of sinking 25 mA and sourcing 15 mA, the 3-state output, which assumes a high or low condition when selected or a floating state when not selected or in a write operation, easily drives a data bus as well as several TTL loads. Specifications for the RAMs, which are manufactured by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 94301, include maximum cycle times of 55 ns and 70 ns for the 2147-3 and 2147, respectively, while typical current requirements in standby mode are 15 mA and 10 mA with 120 mA and 100 mA, respectively, required when the RAMs are active. The devices are packaged in 18-pin ceramic DIPs and operate from a single 5-V $\pm 5\%$ supply over a temperature range of 0 to 70°C. Circle 353 on Inquiry Card

16-Bit DAC Offers 14-Bit Monotonicity

Guaranteed monotonicity in the 16-bit, MN3310 D-A converter (DAC) over the entire 0 to 70°C temperature range is 14 bits. This breakthrough in performance over temperature, claimed by Micro Networks Corp, 324 Clark St, Worcester, MA 01606, results from proprietary thin film resistor technology which is capable of producing DACs and other networks



Sooner or later it was bound to get out.

Yes, the Dumb Terminal™ really does have two smarter brothers.

At first, they weren't quite as well known, because their Dumb Brother's smashing success was stealing the show. Although they had been selling quite well all along, even without getting constant headlines, like their Brother.

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The ADM-2 is also available in a model compatible with your Burroughs TD-800 Series. The ADM-2B. The ADM-2B adheres to the standard Burroughs poll and address line discipline.

On top of all that, we've made the ADM-2 micro-programmable. And taken all the mystery out of the procedure. Which makes user-micro-programmable simple, quick, and cost-effective. The ADM-2's versatility is limited only by your imagination.

You could call the other Smarter Brother, ADM-1, the "with-or-without" terminal. Starting with some pretty smart standard features, like a standard 24-line display, a field protection feature with dual-intensity and switch-selectable operating modes — block mode and conversation mode — you build up from there. With options like a hardcopy printer interface, and display editing capabilities (line insert, line delete, line erase, character insert, and character delete). Just add the options you need, and leave the rest of the "bells and whistles" for someone else. That way, it's more systems adaptable. And it's up to you just how smart you want it to be.

The Smarter Brothers have it all. Intelligence, appropriate functions, and sensible cost-per-performance.

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After all, there's really nothing wrong with exposing your Smarts.



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with resistor-to-resistor tracking of better than 0.5 ppm/°C.

Said to be ideal for applications such as precision servo and control systems, high accuracy function generation, and precision instrumentation, the DAC affords a settling time better than 35 μ s for a full scale change. In addition, it offers a slew rate of 0.5 V, linearity error of $\pm 0.003\%$ FSR, and absolute accuracy of $\pm 0.3\%$ FSR max over the full temperature range. The device

draws typically 270 mW of power and requires a power supply range of 15 to -15 V.

The DAC is constructed using functional laser trimming to eliminate the need for external trimpots. All specifications are met without adjustment; however, gain and zero adjust points are provided for applications requiring very high accuracy. Packaging is in a 24-pin hermetic DIP.

Circle 354 on Inquiry Card

Monolithic ADCs Drive LCDs and LED Displays

All necessary active devices are contained on the ICL 7106, a single monolithic IC. This high performance, low power, CMOS, 3½-digit, dual-slope, autozero, autopolarity A-D converter directly drives a liquid crystal display (LCD) including backplane drive. Similarly, the ICL 7107 directly drives instrument size light-emitting diode (LED) displays without buffering. Together with seven passive components, display, and power supply, either IC can form a complete digital panel meter with automatic zero connection and automatic polarity.

The ICs accept a floating differential input which can have a full-scale input voltage of 200 mV to 2 V by setting the chip's reference voltage to one-half the normalized full-scale input. With an input impedance of more than $10^{12} \Omega$, the devices afford a typical noise-referred-to-input of 15 μ V, a guaranteed zero reading for a 0-V input, and a rollover (+ to - full-scale symmetry) of less than 1 count. Moreover, with a single reference voltage, no adjustment of rollover is required to produce the low rollover value.

Semicustom Chips Offer Full-Custom Features

A typical linear design for the Monochip MO-E and -F semicustom LSI chips can use over 90% of the chip area, reducing the production-cost differential between semi- and full-custom linear ICs. Inclusion of many

Produced by Intersil Inc, 10900 N Tantau Ave, Cupertino, CA 95014, the ICs use the dual-slope integration technique, which affords each device the advantage of noncritical components, high noise and ac signal rejection, noncritical clock frequency, and excellent differential linearity. Additionally, each IC offers guaranteed accuracy of ± 1 count over its entire ± 2000 -count full-scale digital range, a zero width of 0.7 to 0.9 count for a 0 to 1 transition, and true polarity at zero count for precise null detection.

Capable of implementing true ratiometric reading applications over the full-scale input range, the devices contain on-board clock and reference, a digit suppression feature to indicate overrange conditions, and a minus polarity indication. The ICs, packaged in 40-pin plastic or ceramic DIPs, consume less than 40 mW of power at 10 V.

The manufacturer also provides LED and LCD evaluation kits to assist users in evaluating the devices. Besides the ADC, each kit contains all the necessary parts to build a 3½-digit panel meter, except for the power supply required to operate the meter.

Circle 355 on Inquiry Card

types of semiconductor components including lateral npn and small and high current npn (on the -F only) transistors, which also serve as zener and forward-bias diodes; a number of MOSFETs; and base-diffused and pinch resistors enables a wide variety of custom applications for the chips.

The npn transistors, with a useful current range of 0.1 μ A to 200 mA

and a current gain (h_{FE}) of 80 to 300, contain two or four collector contacts for interconnection. High current npn transistors have a 10- μ A to 200-mA useful current range and a 50 to 250 h_{FE} each for high current applications. Still higher current carrying capability is afforded by being able to connect transistors in parallel. With the same current range and an h_{FE} of 5 to 80, pnp transistors on the chip contain split collectors, effectively doubling their usefulness by creating two devices in such applications as current sources and active loads. Finally, the MOSFETs on both chips have a threshold voltage of 4 to 7 V and serve as lateral switches, variable resistances, and current sources.

Both npn and pnp transistors serve additionally as forward-bias and zener diodes: npn types function where reverse voltages below 6 V are found, pnp types where reverse voltages are above 6 V. Similarly, zener diodes, with a breakdown voltage of 6.6 to 8.0 V and a temperature coefficient of 2.55 mV/°C at a 10-mA current, are created from npn transistors by connecting together the emitter and collector to form the zener's cathode. To produce a temperature coefficient close to zero, a zener can be connected in series with a forward-bias diode.

Besides semiconductor devices, the chips contain five values of diffused resistors (200, 450, 900, 1800, and 3600 Ω) with the lowest value part serving as a cross-under or emitter balancing resistor while the larger four, arranged in a 1-2-4-8 ratio, offer a large number of resistance values when connected serially or in parallel. To acquire greatly increased resistance values, the pinch resistors, with a minimum 6-V breakdown voltage, are used.

Produced by Interdesign, Inc, 1255 Reamwood Ave, Sunnyvale, CA 94086, the MO-E chip measures 70 x 70 mils, contains 200 components, and comes in a package with up to 18 pins. The larger MO-F, claimed to be the largest linear chip ever developed, measures 90 x 110 mils, contains 460 components, and is packaged with up to 24 pins. Tooling costs for the chips run \$2800, with prototype chips available four weeks after receipt of tested breadboard design from customer.

Circle 356 on Inquiry Card

Here's how Data General's microNOVA system stacks up against the competition.

microNOVA Processor:

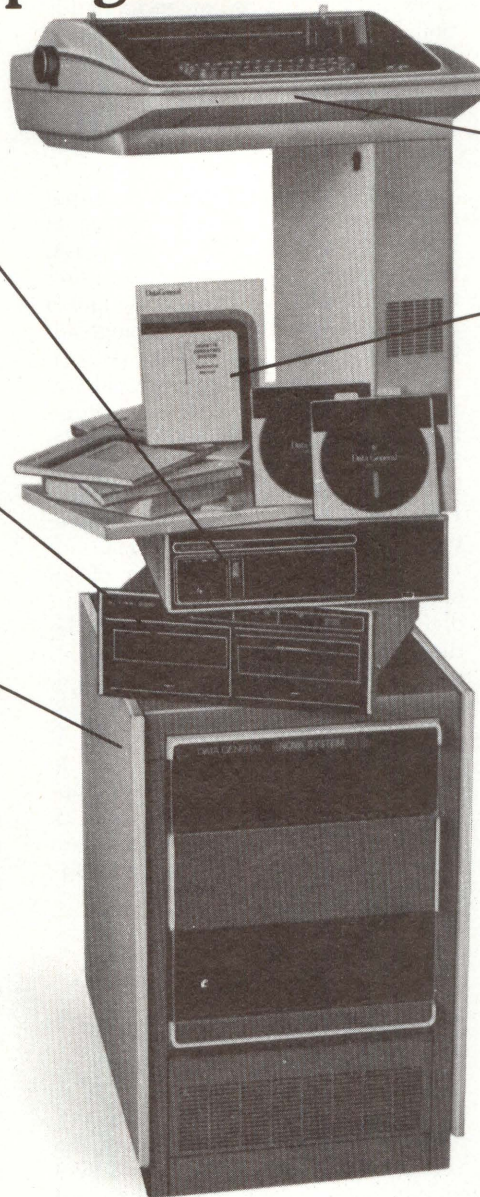
Fully packaged 9-slot micro-computer, 16K words MOS memory, 2.4-microsecond arithmetic operations, hardware stack facility, multiply/divide, DMA capability. Includes RTC, PF/AR and APL. Supports up to 32K words RAM/PROM memory.

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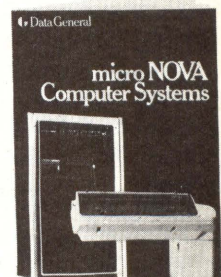
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CIRCLE 93 ON INQUIRY CARD

Wideband Bipolar Log/Antilog Amplifier Has 4-Decade Dynamic Range

Model 2910 bipolar logarithmic amplifier serves as a bipolar or unipolar logarithmic or antilogarithmic amplifier, affording a dynamic range of 80 dB and offering full-scale, large signal, and minimum level frequency response of dc to 10 MHz minimum. The amplifier may be used with an external resistor for a wide variety of input voltages or directly with current source devices.

A product of Optical Electronics Inc, PO Box 11140, Tucson, AZ 85734, the amplifier, with its four decades of dynamic range, serves in such applications as video systems, pulse systems, communication circuits, fast computational systems, and other wide band applications. A specific application uses two of the devices for gamma correction functions in a video amplifier.

Operating from a standard nominal ± 15 V supply over the -65 to 125°C temperature range, the amplifier produces a maximum logarithmic error of $\pm 1.0\%$ of output typical over the 80-dB dynamic range, falling to $\pm 0.7\%$ of output typical over a smaller 60-dB dynamic range. Input voltage for the device ranges from ± 1.0 mV to ± 10 V full scale; while output voltage ranges between ± 100 and ± 400 mV full scale.

Logarithmic or antilogarithmic operation is determined by the pins used for input and output. Similarly, current or voltage input devices are accommodated by connecting to different input pins. Housed in a 16-pin DIP, the unit sells for \$33 in 10-unit quantity.

Circle 357 on Inquiry Card

Low Cost Monolithic V-F Converter Serves Varied Applications

Using combined CMOS and bipolar technology to effect high performance circuits that employ the charge balancing integrator principle, the monolithic VFQ-1 voltage-to-frequency converter affords a 10- to 100-kHz full-scale output frequency available in either pulse or square wave form. It serves such common applications as remote data transmission, high voltage isolation measurement, tem-

perature-to-frequency conversion, long term integration, and voltage-controlled oscillator.

The converter accepts an input current range of 0 to $10\ \mu\text{A}$ with a 500% overrange capability and interfaces to TTL, CMOS, or HNIL. Additionally, it affords linearity, which holds down to 0 output frequency, of typically 0.01 and 0.1% and a maximum 0.05 and 0.25% for, respectively, the 10- and 100-kHz full-scale outputs.

Besides requiring input and output connections and a supply voltage of between ± 4 and ± 7.5 V at 4 mA, the converter externally requires three resistors, two capacitors, and a reference; moreover, if zeroing adjustment is used, a trimming potentiometer and two more external resistors are necessary. Manufactured by Dattel Systems Inc, 1020 Turnpike St, Canton, MA 02021, the device can be configured to operate as either a v-f or f-v converter by the connections made to its external pins.

The converter is made up of an operational amplifier; comparator; digital delay; single-pole, double-throw electronic switch; a divide-by-two circuit; and open-collector npn transistor output drivers which provide a logic high level up to 18 V and afford the converter its flexible interface. Versions -1C and -1K operate over the 0 to 70°C and -25 to 85°C temperature ranges and are available in plastic and ceramic 14-pin DIPs.

Circle 358 on Inquiry Card

Counter Offers Direct TTL/ECL-Compatibility

Optimized for use in ECL and TTL counters, timers, and synthesizers, the SP8735B and SP8736B divide-by-8 circuits operate from dc to 600 and 500 MHz, respectively, with a direct gating capability up to the maximum operating frequency. The dividers, which consume <400 mW of power, are manufactured by Plessey Semiconductors, 1641 Kaiser Ave, Irvine, CA 92714, and require an input clock amplitude of 400 to 800 mV pk-pk. They operate over the 0 to 70°C temperature range.

Binary output and one-of-two carry outputs are TTL-compatible while the second carry output is ECL-compatible. Although the divider's reset input, which clears the device to zero when enabled, is TTL-compatible, the clock input, which is capacitively coupled to the signal source, is gated by an ECL III/ECL 10k compatible input.

Circle 359 on Inquiry Card

Fabrication Technique Facilitates Production

Wafer process technology in which a surface acoustic wave (SAW) device image is stepped and repeated on a mask array makes possible high volume production of SAW devices. Each 2" (5-cm) crystal substrate contains hundreds of devices ready for separation and crystal mounting. Metallic layers of aluminum, chrome, chrome-gold, titanium-gold, molybdenum, polysilicon, tungsten, and other metals are used in these devices.

At present, 0.2-mil metal line and spacing resolution can be achieved with 5000-Å thick metal over 0.25" (0.6 cm) lengths. SAW devices, which serve as analog bandpass filters, transversal filters, and delay lines have been fabricated by the originator of this new technique, Mosfet* Micro* Labs Inc, Penn Centre Plaza, Quakertown, PA 18951, on lithium niobate, bismuth silicon oxide, tellurium dioxide, and quartz crystals as prototypes for other electronic laboratories.

Circle 360 on Inquiry Card

Low Cost ADC Offers Speed and Accuracy

ADC541 series A-D converters, produced by Hybrid Systems Corp, Crosby Dr, Bedford Research Pk, Bedford, MA 01730, provide 8-bit resolution and 10- μs conversion time, and drain a low 700-mW of power using standard ± 15 - and 5-V power supplies. Functioning in data transmission, transducer digitizing, infinite sample and holds, and, because of their small size, in microprocessor applications as well, the converters consist of a precision thin-film DAC, clock, comparator, reference, and successive approximation register.

Externally pin-connectable for three unipolar and three bipolar input ranges, the devices allow user selectable offset binary or 2's complement output coding in bipolar mode and feature a ± 45 -ppm/ $^\circ\text{C}$ temperature coefficient and a 0.1%/yr long-term stability. Furthermore, the three models of the device (-8, C-8, and B-8) are hermetically sealed in 24-pin metal DIPs and operate over the 0 to 70°C , -25 to 85°C , and -55 to 125°C temperature ranges, respectively. The B-8 is processed to meet MIL-STD-883A class B. □

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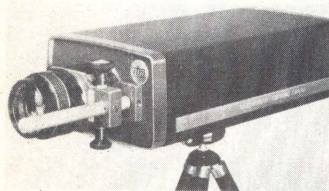
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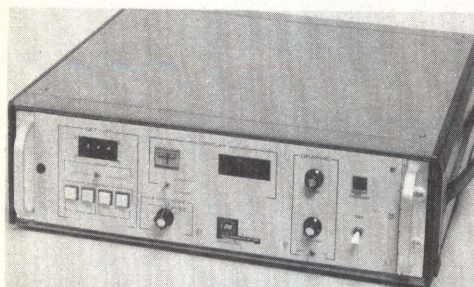
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PRODUCT FEATURE



Optical Data Acquisition System Combines Video and Digital Technologies



Multispectral industrial inspections, nondestructive testing, earth resources and remote sensing surveys, biomedical and radiological analyses: these are just a few of the potential applications for an optical data acquisition system developed by ITM Inc. Typical analyses could involve pattern recognition, integration and differentiation of views, selective enhancement, area measurement, scenic geometric dimensioning, surface and subsurface thermal flow delineation, and similar tasks where optical data must be captured, processed, and displayed.

Subject items for analysis might be as diverse as infrared photographs, blood specimen samples, or

radiographic scans—or even forest fires or oil spills under “live” conditions. In each case, the system combines optical, video, and digital technologies to scan and analyze the chosen subject—or, specifically, a selected area of that subject—and to store the video information for later detailed study.

Spatially distributed scenic data captured with a standard TV scanning action are digitized as 8-bit words, representative of image picture elements or pixels, and transferred directly into a computer or offline memory device. By choosing specific sections of the overall field of view prior to scanning, digital storage requirements are reduced to

that available with a small scale computer.

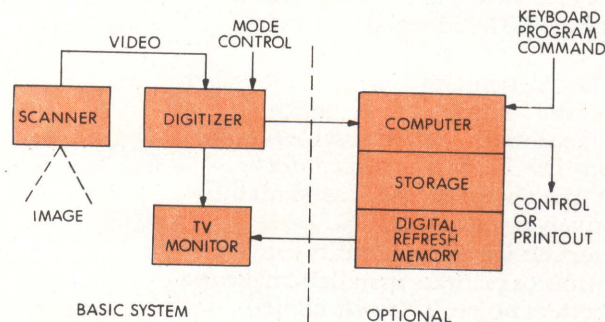
Two major components form the optical data acquisition system: a model 201 series multispectral scanner (camera) and an Arad-50 image digitizer. In addition, a small black and white monitor (diagram) enables the user to monitor the optical field of view and to observe the digitizer's action on the scene. A mini-computer with storage facilities for digitized image data and an output memory for refreshing the processed image data to the display are optional. All but the scanner and digitizer may be stock commercial items.

Detailed System Description

The multispectral scanner utilizes the American standard 525-line TV scanning format but differs from the ordinary TV camera in that it provides a logarithmically corrected gray-scale response for pixel readout in terms of image density. Stability and readout accuracy suitable for digitization are far beyond that available from an ordinary TV camera. The scanner has both internal and external synchronization capabilities and can drive standard recording, analysis, and display devices directly. Scanning synchronization may be provided from an external source such as the digitizer or the computer clock.

Models of the scanner are available for densitometric, ultraviolet radiometric, and near- and far-infrared service. Key features include a 3-decade linear density readout for scenic gray-scale values, stable black-scale reference, high shading accuracy, geometric linearity, and freedom from image retention.

In practice, light emerging from the brightest portion of a 3-decade tonal scene will be 1000 times as in-



Typical image analysis system block diagram. Model 201 scanner and Arad-50 digitizer are key components, TV monitor provides visual display, and computer/memory components are optional.

Our first SBC 80 compatible systems for 1977!

4K to 64K RAM Up to 8K EPROM on one board

Now you can have RAM and EPROM on the same board and buy as much or as little memory as you need. And because our memories use 16 pin memory element sockets you can change your memory when you change your mind.

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Compare these features with our much improved read, write and refresh cycle times and you'll choose MSC first.

16K RAM Version

Up to $16K \times 8$ of RAM and up to $8K \times 8$ of EPROM on the same board.

RAM expandable in $4K \times 8$ increments and EPROM expandable in $1K \times 8$ or $2K \times 8$ increments.

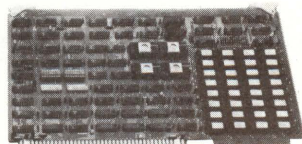
On-board DIP switches to select any of 16 address start locations for RAM and 16 address start locations for EPROM.

Cycle times:
Read, 350 nsec.
Write, 500 nsec.
Refresh, 500 nsec.

Totally SBC 80 and Intellec MDS hardware and software compatible.

Limited one year warranty on parts and labor.

Delivery 30 days ARO.



MSC 4502

64K RAM Version

Up to $64K \times 8$ of RAM and up to $8K \times 8$ of EPROM on the same board.

RAM expandable in $16K \times 8$ increments and EPROM expandable in $1K \times 8$ or $2K \times 8$ increments.

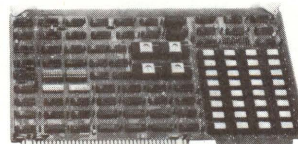
On-board DIP switches to select any of 16 address start locations for RAM and 16 address start locations for EPROM.

Cycle times:
Read, 350 nsec.
Write, 500 nsec.
Refresh, 500 nsec.

Totally SBC 80 and Intellec MDS hardware and software compatible.

Limited one year warranty on parts and labor.

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MSC 4602

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REAL TIME SYSTEMS ENGINEERS

The candidates will review, analyze and propose requirements for common real-time system processor communications and peripherals for retail products. They will interact with other corporate and divisional groups for corporate commonality. They will provide consultation to the system/product designer on industry standards interpretation and adherence needs. Generates guidelines on communications and peripherals usage in Retail Systems.

From 3-10 years experience with a BS in Electrical Engineering, Systems Engineering or Computer Science is required; and MS is desirable. Knowledge of one or more of ANSI (ISO) standards on communications cassette, Disk, File formats, peripheral interfaces, code SETS and E.F.T. is very desirable.

SR. PROGRAMMER ANALYSTS

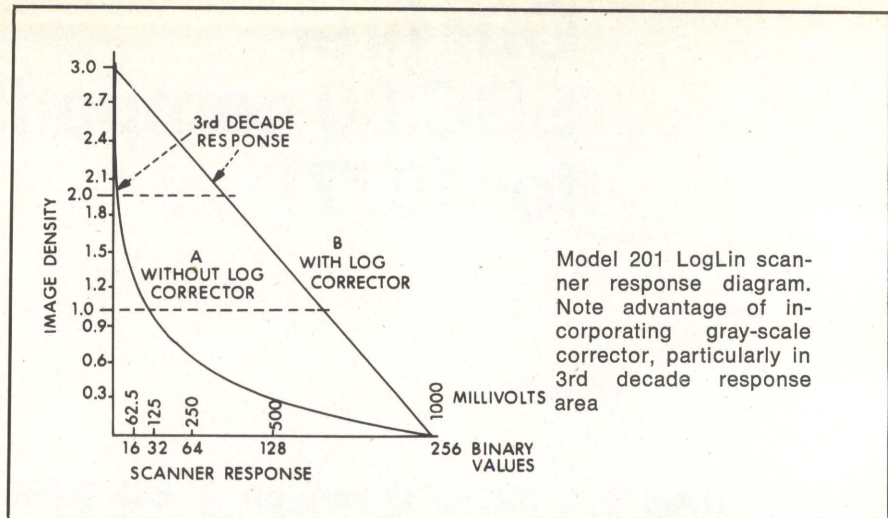
To analyze state-of-the-art software and systems technologies and determine the feasibility of implementing new software techniques on future Point-of-Sale terminal systems. The analysis will involve consideration to the applicability of microprogrammable microprocessors to the requirements of future P.O.S. terminals. Prime areas of concern are implementation of high level languages, operating systems, communications, memory utilization, and diagnostic approaches. A strong computer science training (MS/PhD) and background of 5-10 years experience will qualify you to guide us in software and system technologies for our future terminals.

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tense as from the darkest portion. The high illumination that must be provided for the dark scale rendition then tends to cause image retention on the vidicon target for the brighter areas of the standard TV camera. However, stability and bright scale response of the 201 scanner assure that image retention is negligible and that no appreciable gray-scale shift will be experienced even with wide ranging variations in the average scenic illumination level.

A LOGAMP® gray-scale analog correction module in the scanner provides continuous smooth curve correction response over a 3-decade dynamic scaling range and is vital to the accuracy of the digitization. Image density signal output is maintained to within 0.05 density units (D) accuracy full scale. (Advantage of this scaling corrector is apparent from the LogLin scanner response diagram which is plotted on analog and digital scales.)

Shading error is less than 0.04 D across the central 80% portion of the TV raster and approximately 0.02 D across the central 40%. Target blemishes are less than 0.02 D, resulting in a highly accurate overall densitometric scanner response.

Among the digitizer's programmable features is the capability to outline an area of the picture being scanned for digitization and consignment to the computer. The monitor view permits the user to position the window visually on the scene so as to selectively digitize portions of the view. Once defined and set up by thumbwheel switches on the digitizer panel, window coordinates can be checked by use of a 4-position multi-

plexing switch and a digital readout panel meter.

The area designated by the window, which may be the full scene or a tiny portion of it, will be the only area to be digitized. Alternately, the window dimensions can be commanded by computer software to multiplex data from various portions of the view automatically. Although the data evolution of the scanner is many magnitudes greater than the operational speed of the computer, the digitizer does not require any kind of buffer storage between it and the computer since the digitizer's data selection rate is programmed to be optimal to the absorption rate of the computer.

Data can be digitized and consigned to computer storage automatically by a single command pulse from the computer. Handshake control of the digitizing action is maintained as the continuous data stream is forwarded to the computer. On a priority interrupt, the system remembers its place and automatically picks up and continues the picture digitization action in a subsequent TV frame at a later time.

Price and Delivery

Single unit prices for the model 201E densitometric scanner and the Arad-50 image digitizer, respectively, are \$6800 and \$7850. Quantity discounts are available on both. Delivery is 30 to 45 days ARO. ITM Inc, 680 Main St, Waltham, MA 02154. Tel: (617) 894-1720.

For additional information circle 199 on inquiry card.

NOVA 3* ADD-IN MEMORY.

At 128K x 17, Mostek offers four times more capacity and industry's lowest price.

Mostek's industry-standard 16K RAM technology makes it possible—a super-dense 128K words \times 17 bits on a single card that's completely hardware and software compatible with equivalent Data General* Memory modules and is available in just 45 days.

The MK 8003 series of add-in memory systems has several capacity options. You can choose from 16K, 32K, 64K, or 128K words \times 17 bits, on a single board measuring just 15" \times 15" \times .440.

Board density is just one of the Mostek advantages in Memory Systems. You can also count on value with competitive prices, OEM discounts, and a full one-year warranty on all Memory Systems. Another big advantage is higher system reliability. Mostek memory systems undergo extensive burn-in and testing prior to shipment.

A broad line of memory system products.

In addition to standard add-in memory for other popular mini-computers, Mostek Memory Systems also offers the MK 8000, a 128K \times 24 single-card system. It's pin

compatible with industry standard core and semiconductor systems. And Mostek's 16K dynamic RAMs make available lower power and greater system reliability.

For complete information on Mostek Memory Systems, call Memory Systems Marketing at (214) 242-0444.

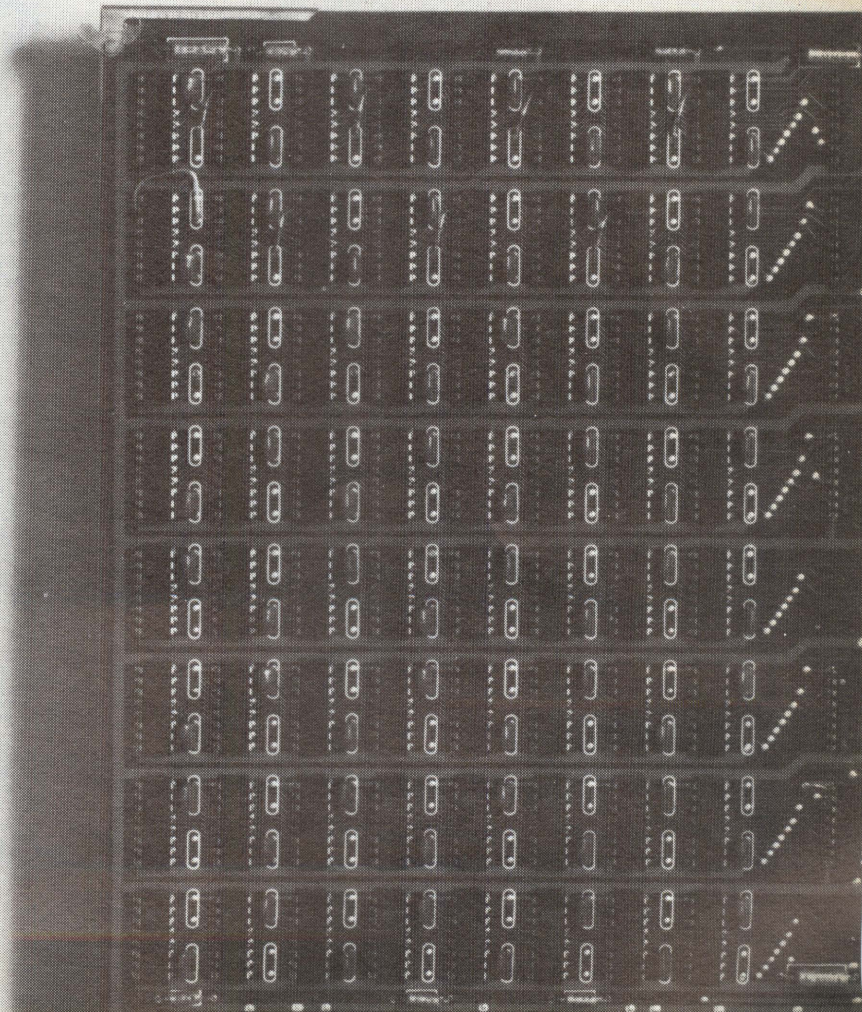
MOSTEK Memory Systems

Setting industry standards in reliability.

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CIRCLE 97 ON INQUIRY CARD



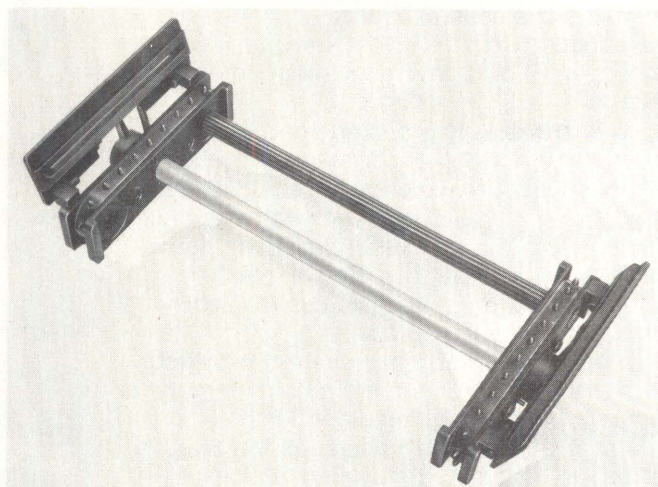
Two-Chip Data Encryptor Device Ensures Security of Message Encryption and Decryption



The CR-100 network encryptor for use in data communications networks or on point-to-point data communications links to provide high level message security utilizes the National Bureau of Standards DES data encryption algorithm under microprocessor control. Two DES chips—each a 40-pin package operating at 1.6 MHz with a data rate of up to 19.2k bits/s—are utilized, allowing full-duplex and synchronous/asynchronous operation. Higher data rates are optional. Device is contained in a secure, 3.5 x 11 x 12" (8.9 x 28 x 30-cm) package for desk or rack mounting. Encryption/decryption key variable is centered by means of a hexadecimal-coded thumbwheel switch under a locked cover requiring dual key entry. Key variable is 64 bits in length including parity bits; parity is checked whenever it is transferred within the unit. **Rockwell International, Collins Government Telecommunications Group**, Cedar Rapids, IA 52406. Circle 200 on Inquiry Card

Plastic, 8-Pull Pin Form Tractor Offers Accurate Paper Feed for High Speed Printers

Available for high speed printers and other equipment, model 880 XACTRON™ tractor uses field proven elements such as a polyimide film belt featuring eight molded-through pull pins and sprocket drive rollers to obtain accurate paper feed. Pin spacings and diameters are held to close tolerances to provide uniform contact with marginally punched paper. One revolution meters 4.0" (10.16 cm) of paper. Features include fast response and low power requirements with low mass belt, and accommodation of wider forms. Belt drive does not stretch under normal operating loads and requires no adjustment; moving parts are made of polycarbonate filled with glass and fluorocarbon—all self-lubricating and noncorrosive. Component is designed to exceed 2 kh MTBF. Std and optional mounting dimensions are offered. **Precision Handling Devices, Inc.**, 63 S Main St, Assonet, MA 02702. Circle 201 on Inquiry Card



Options Offer Additional Ways to Perform Time Measurements With Microprocessing Timer/Counter



Model 9000 microprocessing timer/counter is now available with four added options. Selective gate control (option 05) allows an externally applied pulse to enable channel A and disable channel B for measuring the time interval between any selected number of pulses. Option 06 offers a synchronous window in conjunction with the selective gate control. Channels A and B are enabled, creating a window on time-interval avg measurements, so that a single pulse can be selected and measured. With pulse parameter options 11 and 12, rise time, fall time, and pulse width are measured by pushing a button. For low rate pulses, option 12 lowers the repetition rate from 400 to 75 Hz. Remote programming (06P) allows synchronous window and selective gate control measurement under control of a computer or controller through the GPIB interface. System interfaces include GPIB, parallel BCD, serial ASCII (RS-232-C), or extra high speed. **Dana Laboratories, Inc.**, 2401 Campus Dr, Irvine, CA 92715. Circle 202 on Inquiry Card

If you spend more than 20 minutes picking a P.C. connector

It's your guide to the broadest line of printed circuit connectors made by any single manufacturer. We have just about everything and in more combinations and more depth than anyone — more types of contact terminations, insulator materials, mounting styles, contact designs, types of plating.

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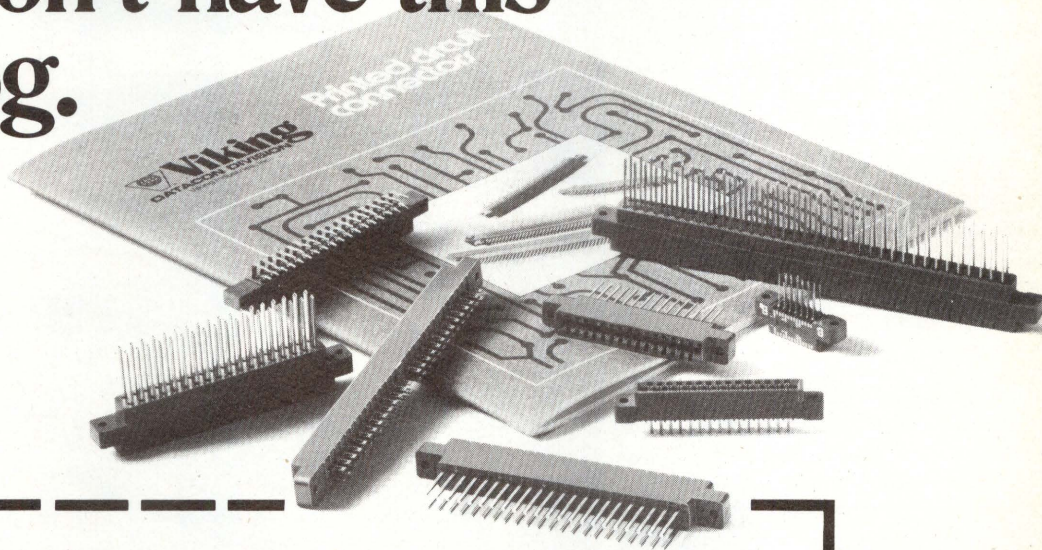
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As you can guess, we have a lot of tooling filed away. Our production engineers have a unique talent at taking an existing bit of tooling, fiddling with it, and turning out a "custom" connector that's exactly what you need. Your extra cost is only a modest set-up charge... a long way from a full retooling cost.

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Chatsworth, CA 91311 U.S.A./ (213) 341-4330/ **DATACON DIVISION**

Why cushion packaging for heavy electronics? Because the bigger they are, the harder they fall.

If the electronic equipment you make is subject to all the usual modes of transportation . . . chances are, it's a good candidate for ETHAFOAM® brand polyethylene foam for cushion packaging.

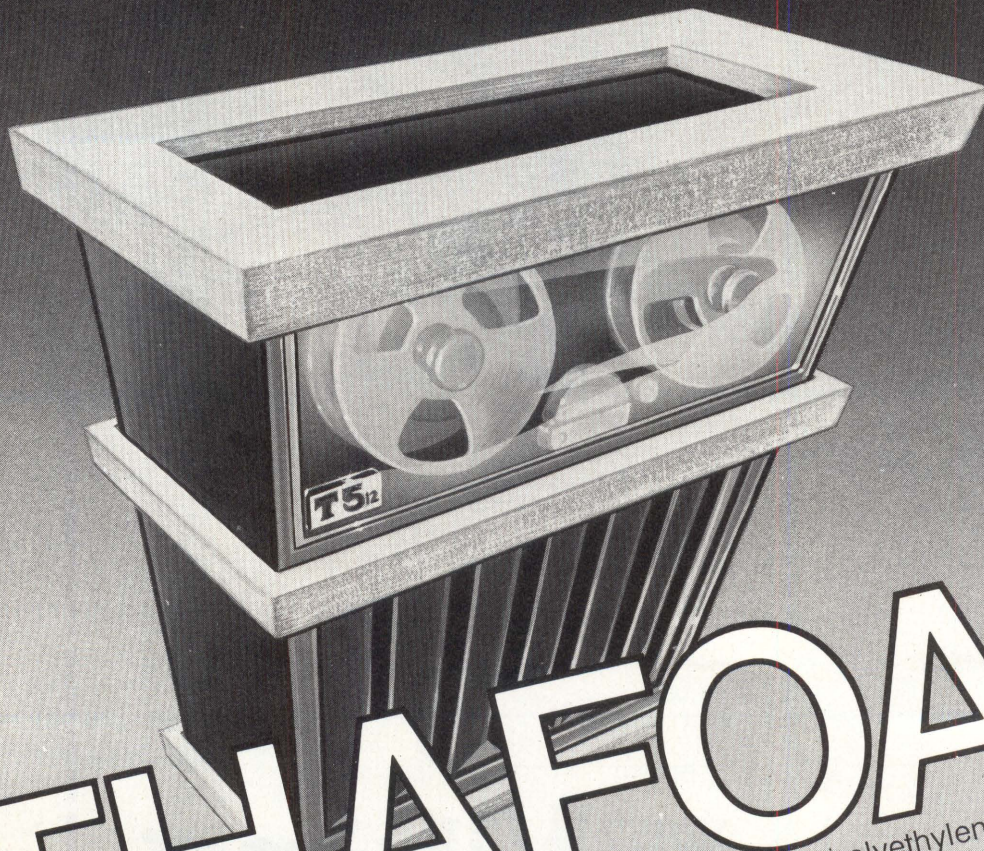
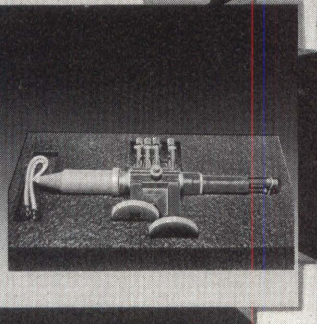
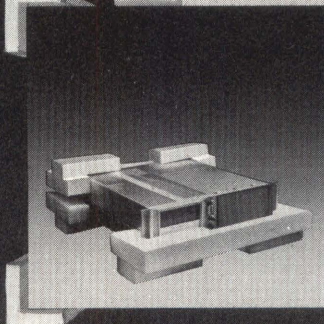
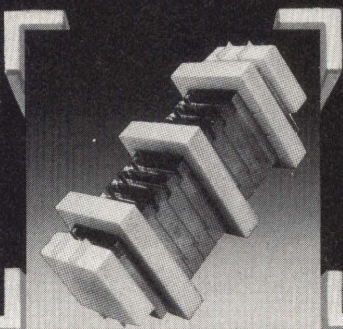
It's by far one of the most efficient packaging materials for protecting delicate electronic gear from hard knocks. Unlike corrugated inserts, ETHAFOAM is a resilient, closed-cell plastic foam. This means it does a better job of protecting from repeated shock, vibration and abrasion. And unlike many molded foam parts, it won't shatter. It boasts excellent recovery, too, returning to shape after impact. Finally, because of its inherent efficiency, you

often need less ETHAFOAM for equivalent cushion protection.

Availability? Fabricators of ETHAFOAM can readily design and deliver the parts your product requires. You'll wind up with packaging that's lightweight and volume-efficient for lower transportation costs. Pleasing in appearance, too.

Cost? Competitive in cushioning, but thanks to its design versatility and other cost-cutting features, ETHAFOAM brand polyethylene foam will probably cost you less in the long run. How's that for delivering the goods.

More information? Check with your nearby fabricator of ETHAFOAM. He's listed on the following page.



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Los Angeles, Zero Manufacturing (213) 846-4191
Menlo Park, Parsons Manufacturing (415) 324-4726
Oakland, Tharco Precision (415) 562-9338
Santa Fe Springs, Republic Packaging (213) 921-0621
S. El Monte, Parsons Manufacturing (213) 443-3277

COLORADO

Denver, Tharco Containers (303) 373-1860

CONNECTICUT

Hartford, Rogers Foam (203) 246-7234
Pawcatuck, M. J. Fox, Div. United Foam
(203) 599-1242

FLORIDA

Hialeah, Republic Packaging (305) 836-1246
Orlando, Military Packaging (305) 855-7860

ILLINOIS

Chicago, Foamcraft (312) 243-6262
Chicago, Republic Packaging (312) 233-6530

KENTUCKY

Lexington, Republic Packaging (606) 254-7715
Louisville, Packaging Services (502) 778-5565

MARYLAND

Glen Burnie, Republic Packaging (301) 766-0126

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Feeding Hills, Can Pak Service (413) 786-0000
Georgetown, United Foam Plastics (617) 662-7600
Lawrence, GSF (617) 475-9616
Mansfield, Keil Brothers (617) 339-8440
Northbridge, Tainer Tech (617) 234-7301
Somerville, Rogers Foam (617) 623-3010
Spencer, Foam Products (617) 885-5353

MICHIGAN

Detroit, Geo. A. Cantrick (313) 343-9100
Fenton, Creative Foam (313) 629-4149
Grand Rapids, Stephenson & Lawyer (616) 949-8100
Royal Oak, Foamade Industries (313) 548-5555

MINNESOTA

Minneapolis, Charles Industries (612) 535-2225
Minneapolis, Federal Packaging (612) 533-1631

MISSOURI

St. Louis, Foam Products (314) 739-8100

NEW JERSEY

Cherry Hill, B. Zeitz & Son (609) 663-5504
Passaic, Rempac Foam (201) 773-8880
Paterson, Crescent Products (201) 278-9368
Piscataway, Paramount Foam Corp. (201) 755-1400

NEW YORK

Buffalo, Bernel Foam (716) 875-2900
Buffalo, Prescottech (716) 822-2100
Long Island City, Styro Sales (212) 786-1791

NORTH CAROLINA

Yadkinville, Hibco Plastics (919) 679-8856

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Barberton, Merryweather Foam Latex (216) 753-0353
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Oklahoma City, Adroit Manufacturing (405) 236-3623

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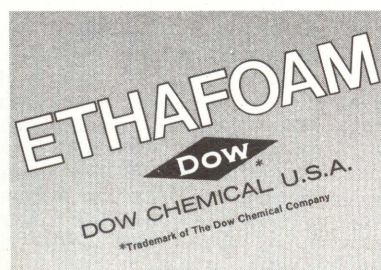
Portland, Republic Packaging (503) 620-0207

PENNSYLVANIA

Philadelphia, Packaging Materials (215) 223-7800

TEXAS

Dallas, Republic Systems (214) 630-7391
Dallas, Wilshire Foam Products (214) 241-4073
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CIRCLE 99 ON INQUIRY CARD

PRODUCTS

2- AND 4-WIRE LOOP MODEM

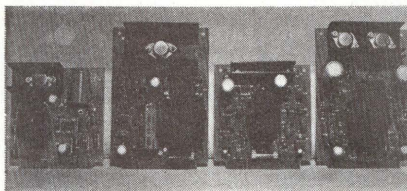


Type 263A transmits and receives digital data over a nonloaded metallic loop at rates of 2.4k, 4.8k, 9.6k, or 56k bits/s. The unit operates in full- or half-duplex mode with 4-wire loops, and in simplex with 2-wire loops. Line signal spectrum complies with requirements of AT&T publication 43401. Interface presented by the modem to the data terminal by 2.4k-, 4.8k-, and 9.6k-bit/s arrangements conforms to EIA RS-232-C and 334. **GTE Lenkurt Inc.**, 1105 County Rd, San Carlos, CA 94070. Circle 203 on Inquiry Card

OPTICALLY COUPLED ISOLATORS

6N138 and 6N139 feature high gain at low input currents, TTL-compatible outputs, 300% min current transfer ratio at 1.6 mA and 400% min at 5.0 mA respective input currents, and 3000-Vdc isolation voltages. They are pin-for-pin compatible with HP 6N138 and -39 isolators and are available in 8-pin DIPs. Isolators incorporate an LED and integrated photo-detector circuit with CTRs, and speeds up to ten times the photodarlington isolators operating at low input currents. **Spectronics, Inc.**, 830 E Arapaho Rd, Richardson, TX 75080. Circle 204 on Inquiry Card

PLUG-IN CARD POWER SUPPLIES

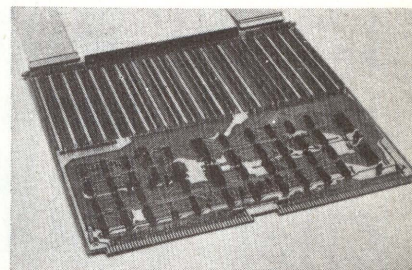


All 34 units are available with single, dual, or multiple outputs and are designed to operate with 110/220-Vac inputs. Outputs may range from 3.6 to 24 Vdc, 100 mA to 3 A, and offer line regulation of $\pm 0.1\%$, load regulation of $\pm 0.15\%$ with ripple, and noise < 5 mV max pk-pk. Series features the use of Mil Spec IC regulator, and foldback current limiting for short-circuit protection with primary fusing. **Computer Power Source**, 370 Park Ave, Worcester, MA 01602. Circle 205 on Inquiry Card

μ C-BASED LABEL PRINTER

Consisting of company's microcomputer, Printronix 300-line/min printer, and CRT, Label/300 prints labels at 300 lines/min with character size variations from 0.166 to 12" (0.42 to 30.48 cm) in block, italic, superscript, and subscript. Options include machine-readable bar code, OCR-A font, and reverse paper feed. Four models are available: 1C is used as a peripheral; 1 and 10 have standalone configurations; and 100 is a standalone system which incorporates H-P 2645 CRT with dual cassettes for increased storage capacity. **Technical Analysis Corp.**, 120 W Wieuca Rd, NE, Atlanta, GA 30342. Circle 206 on Inquiry Card

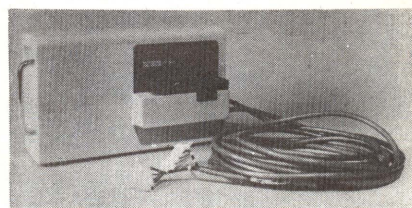
UNIVERSAL INTERFACE MODULES



Providing handshake logic for mini-computers on the bottom half and wire-wrap pins and provisions for mounting up to 114 sockets or ICs on top, module requires only one slot on main-frame. N102-P has necessary receivers and drivers to interface the data bus, busy/done/interrupt control with wire-wrap pin access to all signals; N103-P adds 16-bit I/O registers divided into two 8-bit byte latches. N104-P provides data channel control logic to interface to the NOVA[®] type data channel protocol. **Interconnection Technology, Inc.**, PO Box 126, Accord, MA 02018. Circle 207 on Inquiry Card

SERIAL PAPER TAPE READER

Designed for systems or terminals lacking paper tape input capability and for diagnostic testing of dedicated systems, the PRS01 connects to the serial line of console or terminal or to any 20-mA current loop input. Offered in versions with 300- or 2400-baud transfer rates, device reads 8-level tapes and contains own power supply. Off/on and selection switches for reader or console input permit easy operation. **Digital Equipment Corp.**, Maynard, MA 01754.

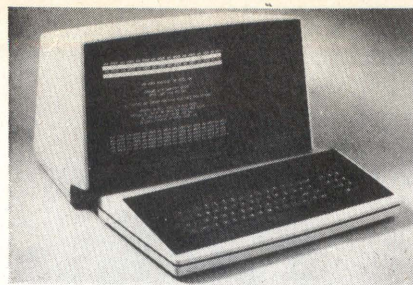


Circle 208 on Inquiry Card

PRODUCTS

CRT TERMINAL

A microprocessor-based CRT terminal, model 400D has a 2k-char memory, 15" (38-cm) diagonal nonglare screen, 72-key detachable keyboard with full 128-char ASCII set, RS-232 data interface, and RS-170 video output. Display format is 24 lines of 80 char with an extra line of hidden memory accessed in roll or scroll modes. Three char accents are blink, dim, and reverse-video. Four case options are available,



as are options of u/lc char, 40-char line, double-height char, and export power. **Ann Arbor Terminals, Inc.**, 6107 Jackson Rd, Ann Arbor, MI 48103. Circle 209 on Inquiry Card

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**PRICES START AT \$240. THE ONLY WAY TO GO FOR
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Data-Control Systems "Loca-Modems" are rugged, reliable data sets specifically designed to access terminals at distances up to 10 miles. *At a fraction of the cost of standard modems.* Available synchronous at 2.4, 4.8, 9.6 and 19.2 kbps (others optional). Or asynchronous up to 1 megabit. Equipped with remote testing switch and transmit, receive and clear-to-send LED's. Full duplex, half duplex, simplex, point-to-point and multipoint operation. Solid, twisted-pair cabling.

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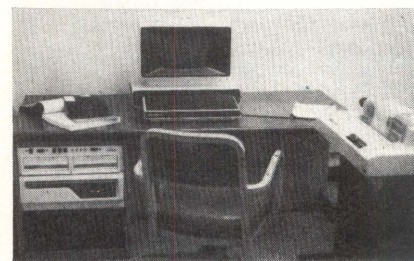
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INSULATION DISPLACEMENT CONNECTORS

For mass termination of flat cables, the PS series of dual row connectors are available in seven contact layouts, 10 position through 50. Termination portion of contact is offset, allowing mass termination of std 0.050" (1.27-mm) spaced round conductor flat cable without prestripping individual wires. Connectors may be applied to cable ends or at any point along cable for daisy-chain applications. Matching straight, right angle, wrappable, and shielded pin headers are available. **ITT Cannon Electric, ETC Terminal Products Unit**, 29000 Aurora Rd, Solon, OH 44139. Circle 210 on Inquiry Card

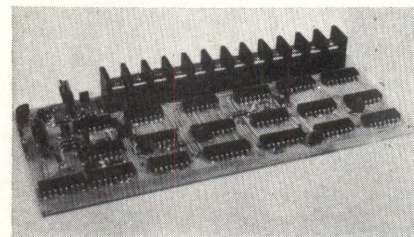
PROCESS CONTROLLER



Designed to handle large industrial control and data acquisition projects, the MC-1 controller consists of a 16k-word CPU, 1920-char CRT terminal, 30-char/s matrix printer, IBM-compatible diskette storage system, and 64-channel analog measurement device which operates at 30 kHz with 12-bit accuracy. I/O interface includes 256 inputs and 128 outputs. The unit's UCP operating system utilizes high level command statements to direct a compiler and to control system functions. **Selanar Corp.**, 3054 Lawrence Expwy, Santa Clara, CA 95051.

Circle 211 on Inquiry Card

SIMULTANEOUS INPUT PROCESSOR



As an interface between high speed detection devices and a counter, the ML33 accepts up to eight simultaneous inputs and process-out counts one at a time at an independent rate. It has storage capacity of 255 inputs in the count register. Processor operates from 10 to 30 Vdc at approx 10 mA; power may be interrupted for 1 ms without losing count. **Anaheim Automation**, 922 Orangefair Ln, Anaheim, CA 92801. Circle 212 on Inquiry Card

Intel delivers PDP-11 memory for people who can't afford to wait.

When you're in a hurry for more semiconductor memory for your PDP-11, call Intel. We deliver memory for the full PDP-11 line. And because we're the largest manufacturer of semiconductor memory in the world, delivery is when you want it.

Why wait? Since you've chosen the leader to supply your minicomputer, it makes sense to go to the leader for memory, too. That's us.

Intel memory systems save you more than time. Our in-1670 add-on memory for the PDP-11/70 is one example. It gives you four times the capacity in the same frame compared to the DEC MJ11-A core memory. And built in Error Correction Code (ECC) and Error Logging improve up-time and reduce maintenance time by automatically correcting and recording single-bit failures and detecting and recording double-bit errors.

For PDP-11 add-in memory go with our in-4711 plug in boards. You'll get memory that's even faster than DEC's. 16K words per hex-wide board. With or without parity. To further expand PDP-11 memory and reduce UNIBUS™ loading choose our in-4011 add-on. With memory management you can expand to 128K words in 16K increments. And since the in-4011 requires only one UNIBUS load, you get added system flexibility.

Get more memory for your LSI-11 and PDP-11/03 in less space with our in-1611 add-in memory. You get up to 32K words, in 8K increments, on a single, two-wide, board. That's up to eight times the memory you get with a DEC board.

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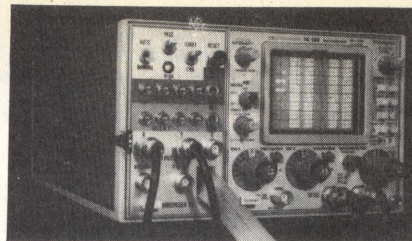
CIRCLE 101 ON INQUIRY CARD

PRODUCTS

LOGIC STATE ANALYZER/ SCOPE PACKAGE

Power of a 32-channel x 64-word logic state analyzer and an oscilloscope are combined in the portable LC-320 package intended for use with micro-based products. In state analyzer mode, 32 leads are connected by a clip cable from the analyzer to the signal buses under test. The instrument can store 64 states of both address and data

buses, and then format the block for display. Switching to the other mode, the unit functions as a standalone, 2-channel, 15-MHz scope. **Scanoptik, Inc.**, PO Box 1745, Rockville, MD 20850. Circle 213 on Inquiry Card

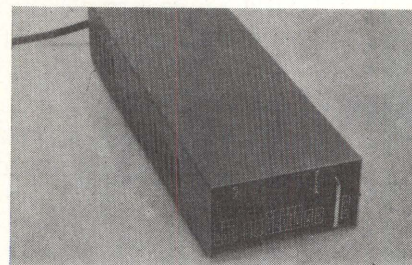


μP-COMPATIBLE TAPE PRINTER

Model DMPT-6 80/96-col text/data printer provides selectable interface functions; parallel ASCII, RS-232/1-loop, and switch-selectable baud rates of 110 to 1200. All needle drivers, character generation, and required diagnostic routines are provided by microprocessor controller. Matrix impact printhead produces 5 x 7 dot matrix characters, and provides full alphanumeric with complete 63-char ASCII set. Printing speeds are as high as 110 char/s. **Practical Automation, Inc.**, Trap Falls Rd, Shelton, CT 06484.

Circle 214 on Inquiry Card

28.8k-BIT/S SYNCHRONOUS LINE DRIVER



The switch-selectable SLD 28.8(M) is capable of transmitting to 6 mi (9.7 km) over nonloaded cable. Multiple data rate permits IBM users to upgrade from 2.4k to 4.8k to 7.2k to 9.6k bits/s, up to the 28.8k max data rate while also allowing a 19.2k half-step speed. Operating over 2- or 4-wire lines, the drivers perform in either half- or full-duplex modes, and in a polled environment. They conform to Bell Spec #43401. **Prentice Corp.**, 795 San Antonio Rd, Palo Alto, CA 94303.

Circle 215 on Inquiry Card

INTELLIGENT TERMINAL WITH FLOPPY DISC



The 8080 microprocessor-based 8035 incorporates CRT terminal, high performance IBM 3740-compatible dual floppy disc subsystem, operating system software, and RS-232-C interface. All system functions are under software control, allowing use for application-specific development of programs. System functions are contained in from 20k to 65k of RAM. FDOS operating system software consists of editor, assembler, and debugger. **Omron Electronics, Inc., Information Products Div.**, 432 Toyama Dr, Sunnyvale, CA 94086. Circle 216 on Inquiry Card

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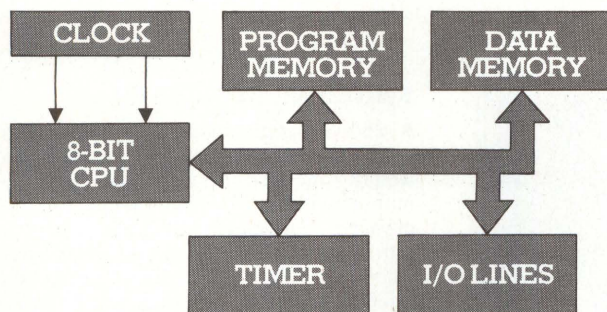
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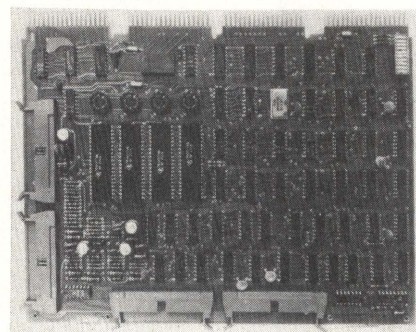
PRODUCTS

PROGRAMMABLE HIGH SPEED PROCESSOR

Operating alone or as a peripheral in minicomputer-based systems, AR-10 has a modular multiprocessor design enabling operations with high throughput and system bandwidth. FFT execution time ranges from 1.45 to 8.5 ms. Subprocessors operate in parallel or interconnected by AR/BUS which performs DMA transfers without cycle stealing. Cross-assembler and linker written in ANSI FORTRAN are combined with hidden pipeline operations for programming. AR/SCAN panel allows operational analysis and program debugging. **Stein Associates**, 280 Bear Hill Rd, Waltham, MA 02154.

Circle 217 on Inquiry Card

4-CHANNEL ASYNCHRONOUS INTERFACE BOARD



QuadrAsync/c is a 20-mA current-loop alternative to DEC's DL-11C and is completely software compatible with that unit. It consists of one quad board and four DEC-compatible male Berg connectors. Operation is full- or half-duplex with transmitter and receiver for each channel operating at the same baud rate. Seven independently selectable baud rates/channel range from 159 to 9600. **Able Computer Technology**, 1616 S Lyon St, Santa Ana, CA 92705.

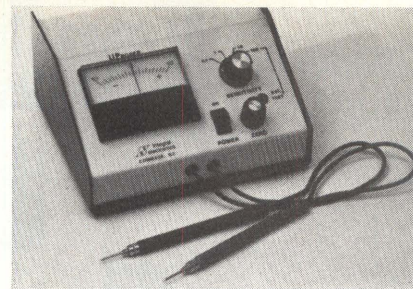
Circle 218 on Inquiry Card

GAS DISCHARGE DISPLAY MOUNTS

Made of nylon per MIL-M-20693A, composition A, Type 1, and UL rated 94 V-2 material, mounting pads are designed to space displays above PCB surfaces. Elevation and protection of the bottom projecting glass seals from contacting boards remove the potential threat of damage. With assured parallel positioning of display to PCB, parallax is eliminated. Funnel-shaped lead entry holes prevent lead strains. Pad serves as pin straightener, guiding leads into the PCB hole pattern. **Bivar, Inc.**, 1617 E Edinger Ave, Santa Ana, CA 92705.

Circle 219 on Inquiry Card

CURRENT TRACING METER



Detection of random solder shorts on PCBs and location of extraneous wires in backplanes and wirewrap assemblies are simplified with aid of Microprober model 42. Spanning a 10,000 to 1 range, the sensitivity permits effective fault isolation of TTL, DTL, CMOS, and ECL circuits. Instrument is powered by a single 9-V battery which provides up to 300 h continuous operation. The unit also serves as a troubleshooter for bus-oriented circuitry. **Integral Electronics Corp.**, PO Box 286, Commack, NY 11725.

Circle 220 on Inquiry Card

SWITCHING REGULATOR

A 250-W supply, which develops high efficiency and reliability in a lightweight package, incorporates a minimum number of components for increased reliability. Features include full rated operation up to 50°C (de-rated to 70°C), built-in protection against overload, short circuits, or over-voltage with foldback current limiting, and a self-cooling design. **Elpac Power Systems**, 3131 S Standard Ave, Santa Ana, CA 92705.

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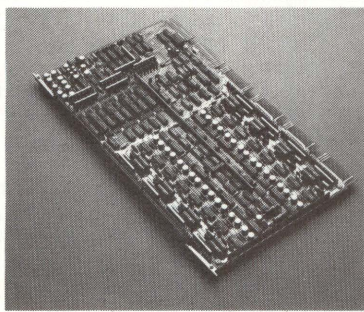
REGISTERED PROTECTIVE CIRCUIT FOR MODEM



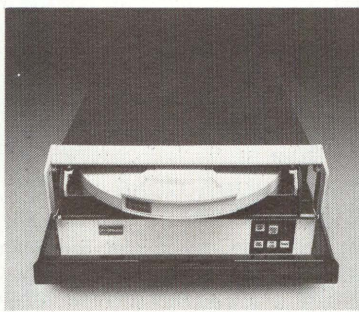
Registered protective circuit permits any dial-up modem to be connected to the DDD telephone network without the Bell direct access arrangement (DAA). Model 7810 is a manual version replacing Bell's CDT DAA; the 7811 is an automatic version replacing Bell's CBS DAA. Both comply with FCC Rule 68 and are registered with the FCC. Features of the 1.75 x 4.375 x 5.5" (4.45 x 11.113 x 13.97-cm) unit include a ring detection indicator and excess power indicator. **Ambac Industries, Inc., Tele-Dynamics Div.**, 525 Virginia Dr, Fort Washington, PA 19034.

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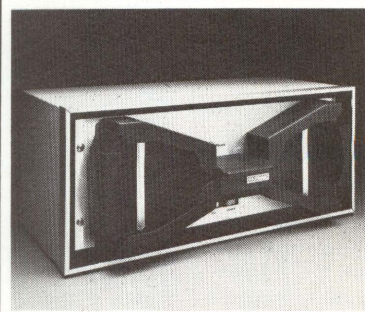
SOMETHING NEW IN MINIPERIPHERALS:



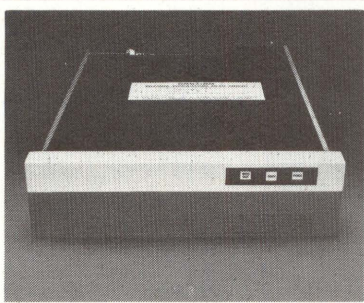
Plessey 8k and 16k plug-in memory modules are fully compatible with your PDP-8, PDP-11, NOVA 2 and NOVA 1200 mini's.



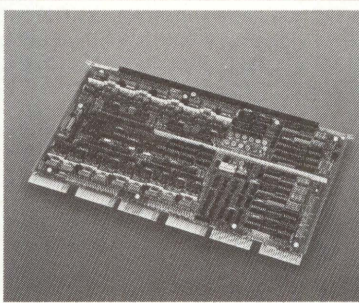
For your PDP-11 and NOVA Series mini's, Plessey can provide plug-in compatible disc systems storing up to 327 megabytes, and 2.5, 5, 10 and 40 megabyte drives.



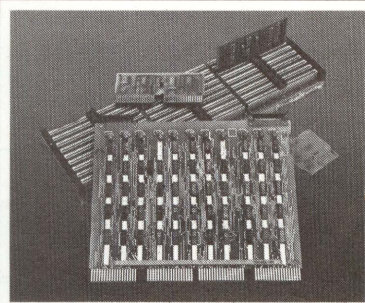
Try a Plessey reader or reader/perforator as a low cost I/O device with your DEC and Data General mini's, or any of the popular microcomputers.



Plessey 3.23, 6.5 and 13 megabyte disc drive systems are plug-in compatible with your PDP-8/A, E, F and M.



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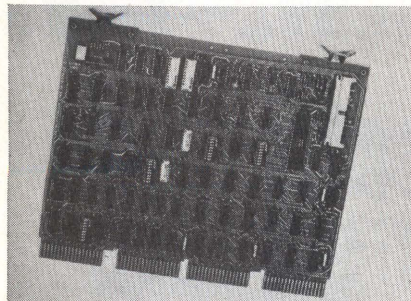
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PRODUCTS

ASYNCHRONOUS SINGLE LINE INTERFACE



As a replacement for DEC's DL11 series, models -01 and -02 of the 2031 series permit interfacing of a CRT or teleprinter at popular baud rate using a single interface card. Baud rates, address selection, and operating mode are all DIP switch selectable. EIA voltage level or current loop are cable connector selectable. Interfaces are fully hardware and software compatible with DEC systems. -02 is available with full dataset control and has baud rates from 75 to 9600. **Gen/Comp, Inc.**, 6 Algonquin Rd, Canton, MA 02021. Circle 223 on Inquiry Card

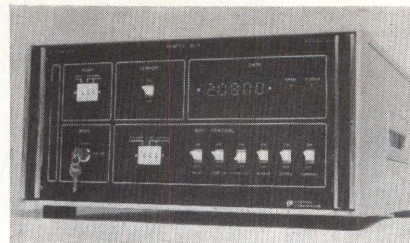
ORIGINATE/ANSWER ACOUSTIC TELEPHONE COUPLER

Enabling remote conversational terminals to be used for both computer time-sharing and message communications, the 702B serves as either originate or answer coupler. Since outputs from both interfaces are available simultaneously, a single coupler can drive a CRT display or other EIA interfaced device, while using a teleprinter for hardcopy recording of information displayed; or provide conversational capability for plotters and card readers with hardcopy tabulation and verification of data. **Omnitac Data**, 2405 S 20th St, Phoenix, AZ 85034. Circle 224 on Inquiry Card

JUMBO SILICA CORE OPTICAL FIBERS

Two pure fused silica step index fibers with attenuations of 3.5 and 2.5 dB/km have 10- and 15-mm min bend radii, respectively, suiting them for UV and IR light transmission and replacement of bundles. Fiber strengths are approx 50 and 200 lb (23 and 91 kg). The 300- μ m dia core fiber has a 440- μ m OD silicone cladding and 650- μ m OD tefzel jacket; the 600- μ m dia core has 750- μ m OD silicone and 1060- μ m OD tefzel. **Quartz Products Corp.**, 688 Somerset St, PO Box 628, Plainfield, NJ 07061. Circle 225 on Inquiry Card

REMOTE MULTIPLEXER UNIT



RIPDL intelligent process data terminal communicates with the central controller of series 2000 via shielded cable, twisted pairs, phone lines, and other communications links. Containing control circuitry and conditioning to accept input directly from std industrial transducers, it uses reed relay multiplexing with integrating type A-D conversion and accommodates from 10 to 100 input channels, expandable in increments of 10 to 20 inputs. **FX Systems Corp.**, 77 Cornell St, Kingston, NY 12401. Circle 226 on Inquiry Card

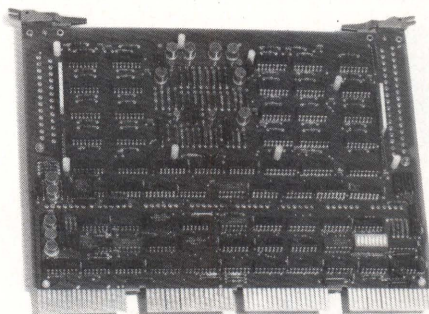
PERMANENT MAGNET SYNCHRONOUS MOTORS

Duty Master[®] P-M synchronous motors are stocked in 1/2-, 1-, and 2-hp sizes. Rotor "poles" are self-excited by means of permanent magnets embedded in the rotor core to achieve higher efficiencies and power factors. Usable on any inverter, PWM or VVI, the motors, which require less kVA/hp, are available in the 140T frame construction using std induction components. They offer precise open-loop speed regulation (zero slip), 4-pole design, and frequency range to 200 Hz max. **Reliance Electric, Motors Div.**, 25001 Tungsten Rd, Cleveland, OH 44117. Circle 227 on Inquiry Card

LSI-11 CORE MEMORY 8K WORDS

The MM-1103 offers double the memory capacity for the same size and power as the DEC MMV-11A core memory.

TOTAL LSI-11 HARDWARE AND SOFTWARE COMPATIBLE



MM-1103

8K x 16

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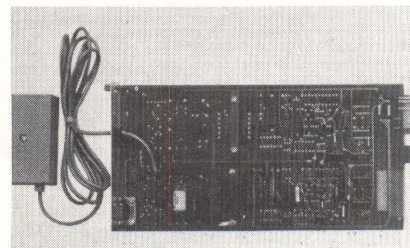
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DATA ACCESS ARRANGEMENTS



Single-channel (VA851) and dual-unit (VA852) data access arrangements meet or exceed requirements of FCC Rule 68. Units directly connect to Bell-type 97A universal data jack (RJ41S) or type 97B programmable data jack (RJ45S). Transmit level control circuit continuously monitors the modem's output level, and automatically reduces the level to protect the line. Circuitry is mounted on a 6.375 x 13" (16.19 x 33-cm) PCB which occupies two slots in a std chassis. **Vadic**, 505 E Middlefield Rd, Mountain View, CA 94043. Circle 228 on Inquiry Card

The new generation of Diskette Drives is here and under control.

PerSci has it—a family of diskette drives “design-years” ahead of competitive drives—now available in complete low cost subsystems for interface to 8080, 6800 and other major microprocessors.

The Highest Performance Diskette Drives:

PerSci diskette drives, both single and dual head units, offer a combination of performance features unique in the marketplace while still maintaining compatibility in existing systems:

- ☐ Voice coil positioning for access speeds seven times faster than competitive drives (76 tracks in 100 ms)
- ☐ A low power all DC system reduces cost and assures high reliability
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The Most Powerful Diskette Drive Controller

The PerSci Model 1070 Diskette Drive Controller puts the advanced performance of PerSci drives to work in microprocessor based systems. An IBM format compatible, “intelligent” controller, the Model 1070 will handle from 1-4 drives with minimum demand on the host system.

In fact, with addition of a power supply and keyboard to the PerSci subsystem, the user can perform many floppy disk routines without additional hardware or software.

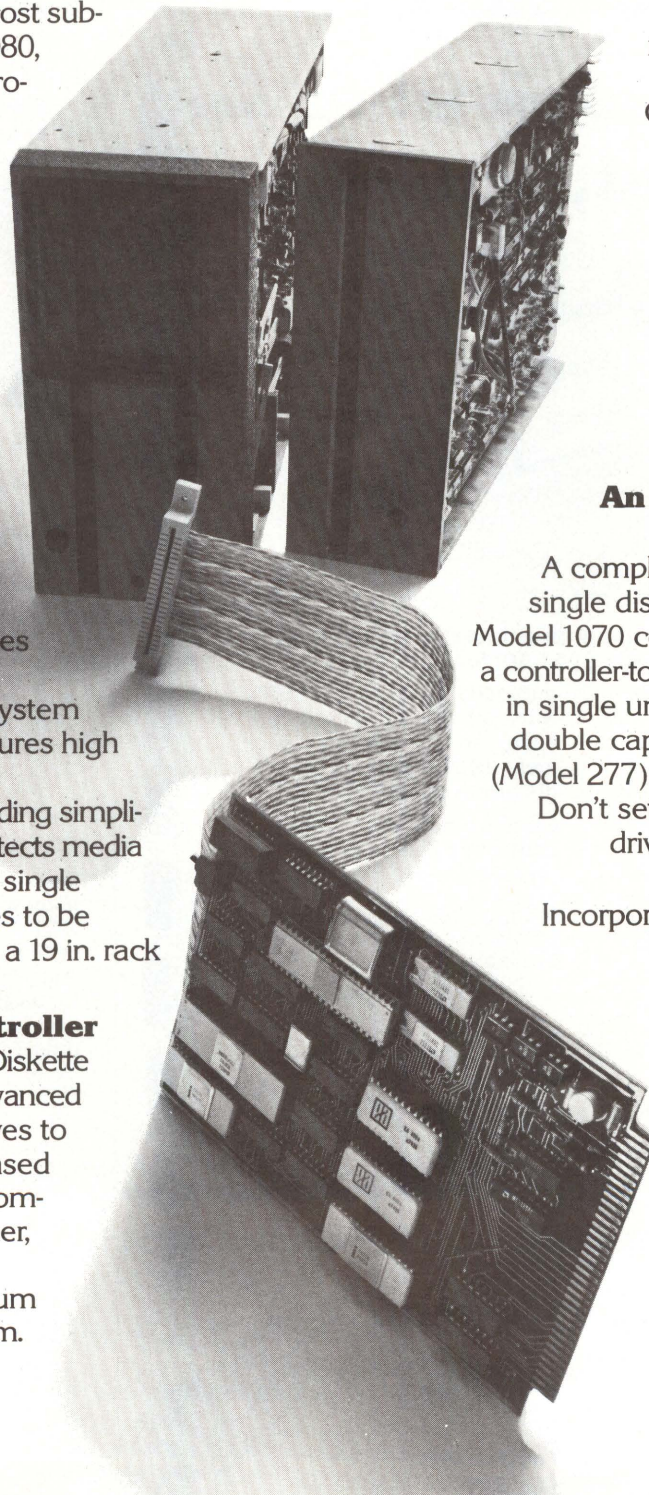
Controller features include:

- ☐ 8080 microprocessor
- ☐ Formatter/control IC
- ☐ 4K disk operating system
- ☐ 1K data buffer
- ☐ 8080 or 6800 microprocessor interfaces
- ☐ RS-232 serial interface optional
- ☐ IBM data format

An Economical Diskette Drive Subsystem

A complete subsystem including a single diskette drive (Model 70), the Model 1070 controller with interface and a controller-to-disk-drive cable is available in single units or OEM quantities. For double capacity, a dual diskette drive (Model 277) subsystem is also available.

Don't settle for yesterday's diskette drive. Get the new generation under control from PerSci, Incorporated, 12210 Nebraska Ave. W. Los Angeles, CA 90025 (213) 820-3764



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PRODUCTS

1200-BAUD DATA COMMUNICATIONS PRINTER

Added to the line of electrosensitive nonimpact high speed printers is the COMM 1200 which operates asynchronously at speeds up to 500 char/s. The communications device measures 19 x 14 x 6" (48 x 36 x 15 cm) and weighs 25 lb (11 kg). Handling 1200-baud transmissions, the printer features self-threading power feed and built-in



self-test. Companion models are KSR and ASR versions. ASCII coding is std with APL, EBCDIC, and Baudot optional. **Scope Data, Inc.**, 3728 Silver Star Rd, Orlando, FL 32808. Circle 229 on Inquiry Card

INTERACTIVE DISPLAY TERMINAL

Compatible with Burroughs computers and equipped for the Burroughs network polling environment, ADM-2B is switch-selectable for operation in two modes. In one, it functions as a std ADM-2. In the other, it is a TD800-series compatible polling unit which adheres to Burroughs poll and address line protocols, provides forms mode for field protection, and has full text and editing features, and eight automatically set status displays. **Lear Siegler Inc., Electronic Instrumentation Div.**, 714 N Brookhurst St, Anaheim, CA 92803. Circle 230 on Inquiry Card

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ALPHANUMERIC DISPLAY TERMINAL



As an alternative to a CRT, the Transactor I data terminal consists of a single line 32-char gas discharge display with 5 x 7 dot matrix, and 53-key TTY-style keyboard. RS-232 or 20-mA current loop interface attaches to most computers. Selection of operating mode includes 110- to 9600-baud rate, full- or half-duplex, even/odd/no parity, five to eight data bits, and one or two stop bits. Unit measures 6 x 15 x 11" (15 x 38 x 28 cm). **Computerwise, Inc.**, 4006 E 137th Terrace, Grandview, MO 64030. Circle 231 on Inquiry Card

CRT TERMINAL

Performing intelligent standalone functions with 4k-word storage requirement, MCT1 has a keyboard with up to 84 stations, 12" (30.48-cm) diag display, and data transmission rates from 50 to 38.4k baud serial and 10k char/s parallel. It is available as p/ROM pre-programmed terminal supporting up to 3k of internal program, 1k of program storage, and 4k of internal data storage. Synchronous, asynchronous, and isochronous data exchanges are available. **Megadata Corp.**, 35 Orville Dr, Bohemia, NY 11716.



Circle 232 on Inquiry Card

\$74.95 **JL** SOURCE.

It's CSC's DP-1: the automatic signal source that cuts hours from trouble-shooting TTL/DTL, CMOS and other popular logic circuits.

This compact, circuit-powered unit lets you inject signals at key points to test digital circuits with fast stimulus-response troubleshooting techniques. Just set a switch to the proper logic family; connect two clip-leads to the circuit's supply, and touch the DP-1 probe to a node. It automatically senses the circuit's condition (high or low state) and produces an opposite-polarity pulse of the proper level. That's all there is to it!

Versatility-flexibility. Select single-pulse or 100 pulse-per-second operation with the handy pushbutton control. A LED indicator signals single-shot or continuous mode. DP-1 can also be connected indefinitely, presenting a 300K impedance to the circuit under test. Short circuits can't harm it, even over prolonged periods. It's also protected against overvoltage up to 25V and reverse-polarity up to 50V.

For all its versatility, portability, operating ease and compact size, DP-1 is priced at only \$74.95—a fraction of what you'd expect to pay for a precision digital pulse source. See your CSC dealer today. Or call 203-624-3103 (East Coast) or 415-421-8872 (West Coast) for the name of your local stocking distributor and a full-line catalog.

Logic family switch—Sets proper pulse level for TTL/DTL or CMOS families.

Rugged, high-impact plastic case—Built to take it... in the lab or in the field.

Protected—Features built-in short-circuit, overvoltage and reverse-polarity protection.

Operating mode pushbutton—Selects single-shot or 100 pps operation.

LED Pulse indicator—Monitors operating mode.

Interchangeable ground leads connection—provide ground-side input connection, where desired, via optional cables.

Interchangeable probe tips—For greater versatility. Straight tip supplied; optional alligator clip and insulated quick-connecting clip available.

Plug-in leads—24" supplied, with non-corrosive nickel-silver alligator clips.

SPECIFICATIONS

Tri-state-output—DP-1 is isolated from circuit under test: $Z \geq 300K$

Auto-polarity pulse sensing—DP-1 automatically produces proper polarity pulse for circuit under test: logic "0" level produces a "1" pulse; logic "1" level produces a "0" pulse

LED indicator—flashes once for single pulse; stays lit to indicate pulse train

Short-circuit protection—can pulse into short circuit continuously

Power—overvoltage protected to 25V, reverse-voltage protected to 50V; voltage range 4-18V, 30mA max.

Pulse modes—Single pulse; press pushbutton for one sec. or less. Pulse train (100pps): hold pushbutton down

Pulse specs	TTL	CMOS
Pulse width	1.5usec \pm 30%	10usec \pm 30%
Fan out	60 loads	
Sink and Source	100mA source to 3.5V; sink to 6V	50mA source to logic 1; sink to logic 0
T_r	100nsec	100nsec
T_f	one TTL load, 500nsec	100K load, 8nsec

* T_r is directly proportional to load resistance

Dimensions (l x w x d) 5.8 x 1.0 x 0.7" (147 x 25.4 x 17.8mm)

Weight 3 oz. (.085kg)

Power Leads plug-in 24" (610mm); color coded insulated clips; others available

ACTION	MOMENTARY PRESS OF PUSH-BUTTON	RELEASE PUSH-BUTTON	CONTINUOUS PRESS OF PUSHBUTTON (OVER 1 SEC.)
LED	FLASHES	OFF	ON
OUTPUT	DP-1 SENSES LOGIC "1" (HIGH), PRODUCES "0" PULSE OR 100 PPS PULSE TRAIN		
	LOGIC 1		
	LOGIC 0		
	DP-1 SENSES LOGIC "0" (LOW), PRODUCES "1" PULSE OR 100 PPS PULSE TRAIN		
	LOGIC 1		
	LOGIC 0		

NOTE: SEE SPECIFICATIONS FOR DUTY CYCLE

CONTINENTAL SPECIALTIES CORPORATION



44 Kendall Street, Box 1942, New Haven, CT 06509
203-624-3103 TWX 710-465-1227
West Coast: 351 California St., San Francisco, CA 94104
415-421-8872 TWX 910-372-7992
Great Britain: CSC UK LTD.
Spur Road, North Feltham Trading Estate,
Feltham, Middlesex, England.
01-890-8782 Int'l Telex: 851-881-3669

CIRCLE 107 ON INQUIRY CARD

NEW DP-1!

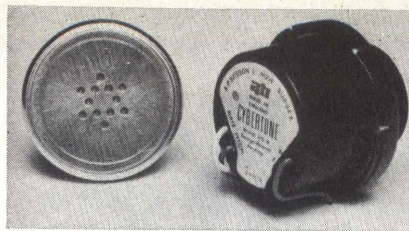
*Manufacturer's Recommended Resale

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PRODUCTS

AUDIBLE SIGNAL/ ALARM DEVICE

For overcoming high noise operating ambients, the MK2 Cybertone[®] offers increased sound power level capability and decreased energy requirement. When used with the "snap-in" horn, a sound pressure level of 95 dBA at 1 m avg relative to 2×10^{-4} dyne/cm² in free field conditions is produced. It provides selectable, programmable, and



audible combinations of 10 different sweeping and continuous sounds, operating on 12 Vdc, $\pm 25\%$ with typ current drain of < 25 mA. **CyberSonic Div, C. A. Briggs Co**, PO Box 151, Glenside, PA 19038.

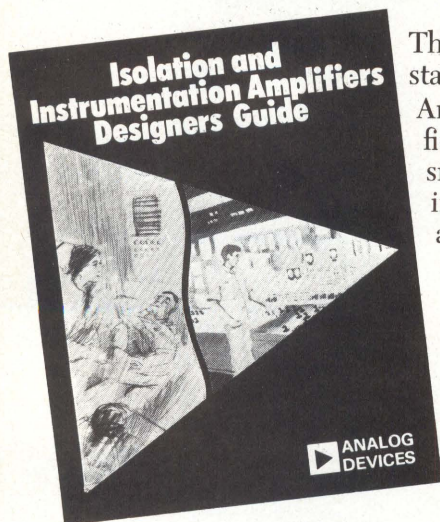
Circle 233 on Inquiry Card

REMOTE DIGITAL DISPLAYS

For use as primary displays in systems that provide parallel BCD data, or as secondary displays when driven by DPMs, frequency meters, or event counters, remote displays interface with these products to provide digital readouts at other than primary locations. Units are available with 0.55" (1.39-cm) planar gas discharge displays in 4- and 5-digit models, and also with 0.6" (1.5-cm) high brightness LEDs in 3½- and 4½-digit models. **Electro-Numerics, Inc**, 1811 Reynolds St, Irvine, CA 92714.

Circle 234 on Inquiry Card

If you have trouble isolating your inputs from your outputs read this book.



This FREE book shows you how to stay out of trouble with low cost Analog Devices isolation amplifiers. Including our latest version, the 286J which offers improved performance for applications in instrumentation, industrial and bio-medical applications. This new design features multi-channel capability for applications in multi-channel data acquisition systems ranging from 2 to over 1000 isolated data points. (\$37 in 100's)

ANALOG DEVICES

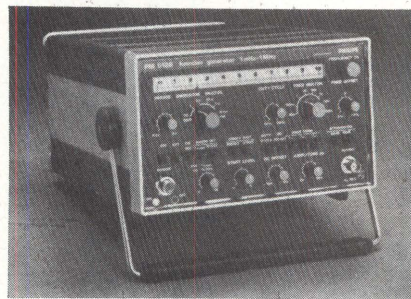
P. O. Box 280 Norwood, MA 02062

Please send me your FREE "Isolation and Instrumentation Amplifiers Designers Guide" and 286J data sheet.

Name _____
Title _____ Telephone _____
Company _____
Address _____
City _____ State _____ Zip _____

CD-10

LOW FREQUENCY FUNCTION GENERATOR



The PM5129 generator with an output from 1 mHz to 1 MHz has low distortion sine, square, and triangle waveforms that can be varied in amplitude, frequency, dc level, and duty cycle. Output frequency is set by a linear scale over eight ranges. Single-shot outputs may be initiated by pushbutton control, variable "peak-level" control, or external TTL signals. In burst mode the number of cycles in each burst can be varied by the period control over a 10 to 1 ratio. **Philips Test & Measuring Instruments, Inc**, a North American Philips Co, 85 McKee Dr, Mahwah, NJ 07430.

Circle 235 on Inquiry Card

PORTABLE 3½-DIGIT RMS DMM



A portable rms-responding DMM with a sensitivity of 10 mV full scale, model 3028B is a 3½-digit multimeter. It has a 10-μV resolution, a 0.43" (1.09-cm) bright orange LED display, and can measure to 10 mΩ. Full emi shielding, rms responding ac ranges, advanced ohmmeter circuit functioning on all ranges, and MTBF >18k hours are std. Also included are overload protection on all ranges and a resettable circuit breaker for protecting current ranges. **Ballantine Laboratories, Inc**, PO Box 97, Boonton, NJ 07005.

Circle 236 on Inquiry Card

A software development breakthrough.



FORTRAN compiler and relocatable macro assembler in a new custom software system for micros.

Now it's easier than ever to create smooth running custom software for PCS SuperPac 8080 A-*based microcomputers. And it takes less time, too. With SPDS. The SuperPac development system.

SPDS has resident software you'd expect to find only in minis. Like a FORTRAN compiler option for fast, easy programming in a language your programmers already know (look for BASIC soon). A cross-reference generator that lists constants, labels and addresses and really saves time when you're moving segments around. A relocatable assembler with full macro capability. And an up-down loader for directly loading software into a target system up to 1,000 feet away and calling it back to the development system

whenever you need it.

Choose the hardware tools you need. A desk console and dual floppy are standard. From there it's up to you. EPROM programmer, CRT terminal, choice of two line printers and paper tape reader are optional.

SPDS for SuperPac microcomputers. It's a software development breakthrough. From Process Computer Systems, of course. The full service microcomputer manufacturer.

* And, soon, for our new Z-80 based micros.

Tell me more. ☐ SPDS ☐ SuperPac ☐ Please have salesman call.

Attach your business card here.



Success is PCS.

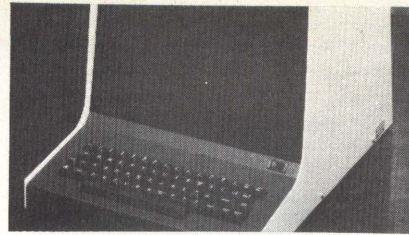
Process Computer Systems, Inc.
750 North Maple Road, Saline, Michigan 48176
313-429-4971 TWX 810-223-8153

CIRCLE 109 ON INQUIRY CARD

PRODUCTS

INTELLIGENT TERMINAL MODULES

Hardware features of the MAS/T2 modules for CRT terminal applications include a 12 or 15" (30- or 38-cm) CRT displaying 24 lines of 80 char, 5 x 7 or 7 x 9 dot char matrix, and 64- to 128-char set. Baud rates are selectable to 9600. RS-232-C and 20-mA interfaces and 63- to 79-key keyboard are std. Among firmware features are all cursor



functions, remote cursor placement and readback, fixed or programmable tab, and automatic line feed. **Micro Application Systems, Inc.**, 4345 Lyndale Ave N, Minneapolis, MN 55412. Circle 237 on Inquiry Card

PROGRAMMABLE DATA COUPLER

Designed for use as standalone packages, the 1692 series of data couplers permit interconnection of customer-provided equipment and switched communications networks, as well as modems with telephone company facilities, according to FCC Rule 68. Automatic level control of transmit signals via a sensing resistor associated with network lines, multidirectional mounting, dc isolation, and surge and spurious voltage protection are std. Switch hook indication and self-test capability are also available. **Harvey Hubbell, Inc., Pulsecom Div.**, 5714 Columbia Pike, Falls Church, VA 22041. Circle 238 on Inquiry Card

The broadest line of Cartridge Tape & Storage Systems



PDP-11
LSI-11
NOVA
ROLM

CARTRIDGE TAPE DRIVE THE MODEL 650 PROVIDES:

- 30 IPS Read/Write, 90 IPS Rewind/Search
- 48,000 Bits/Sec Transfer Rate
- 2.5+ Megabytes per cartridge
- Small Size—Rugged Design

TAPE STORAGE SYSTEMS

- Model 2200—1 or 2 Tape Drives in 5" package
- Model 2400—Up to 8 Tape Drives in 9" package
- Model 2710—Portable Recording System with up to 2 Drives
- Model 86008 Formatter—Used in all Tape Storage Systems. Complete ANSI compatibility with powerful data handling features.

INTERFACES

All tape systems are available with the following controllers: PDP-11/LSI-11/NOVA, ROLM/INTERDATA/ALTAIR/8080/RS232/NTDS.

For more information, call Leon Malmed, Sales Manager

Qantex DIVISION
NORTH ATLANTIC INDUSTRIES, INC.

200 TERMINAL DR., PLAINVIEW, NEW YORK 11803 • 516-681-8350 • TWX: 510-221-1879

TRIPLE OUTPUT DC-DC CONVERTERS

Packaged in 6 x 4 x 2.25" (15 x 10 x 5.7-cm) modules, providing power density of 2 W/in³ (0.1/cm³), 3A series models include 3AD5-12, with 28-Vdc input, 5 V at 10 A and ± 12 V at 2.5-A output; D5-15 with 28-Vdc input, 5 V at 10 A and ± 15 V at 2-A output; E5-12 with 48-V input, 5 V at 10 A and ± 12 V at 2.5-A output; and E5-15 with 48-Vdc input, 5 V at 10 A and ± 15 V at 2-A output. Min efficiencies of 110-W units range from 66 to 68%. All outputs are fully regulated and overcurrent protected. **Etatech, Inc.**, 187-M W Orangerthorpe, Placentia, CA 92670. Circle 239 on Inquiry Card

IBM-COMPATIBLE 2-SIDED FLOPPY DISC HEAD

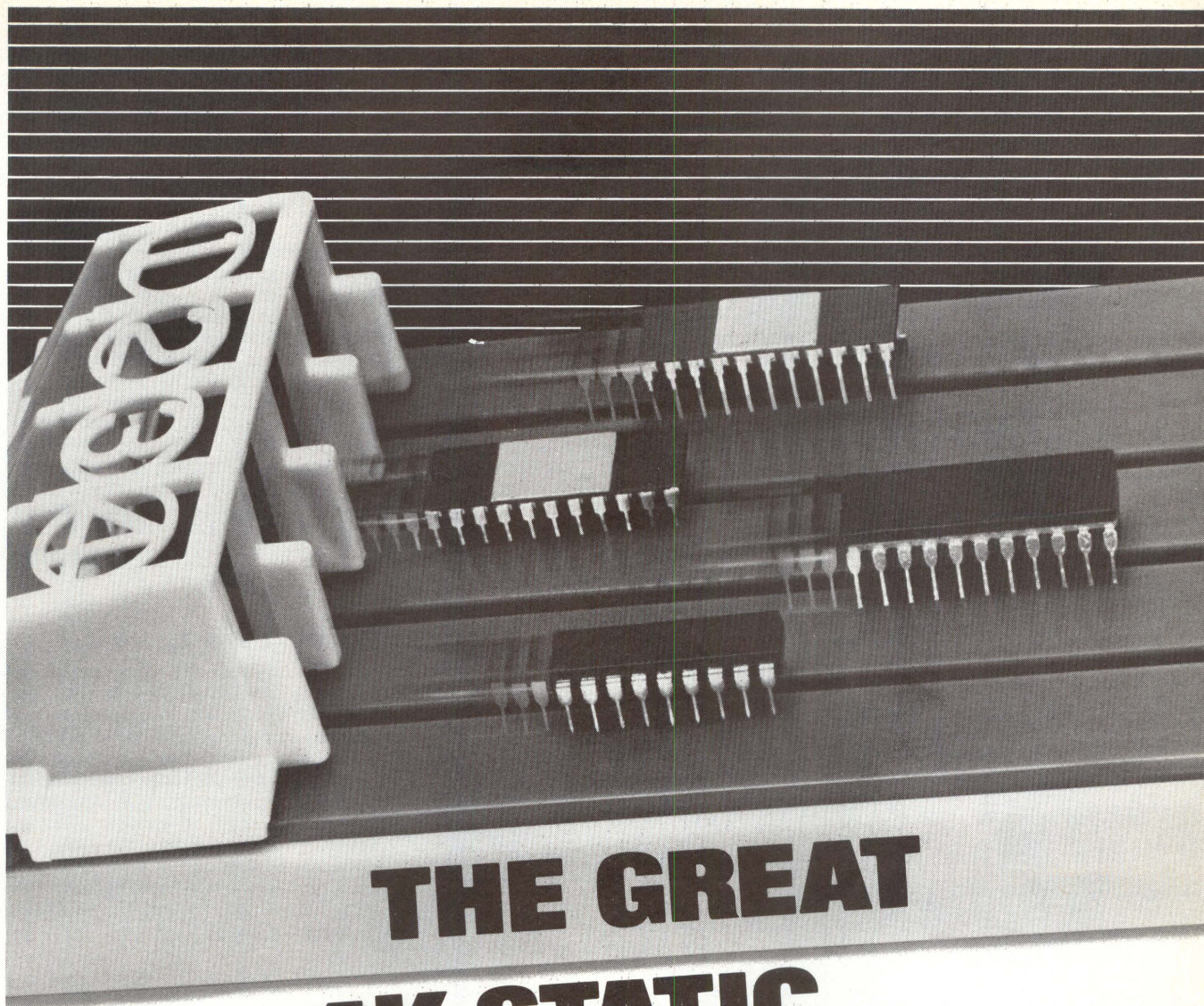
A double-sided ferrite recording head for floppy disc drives, series 200 is compatible with the IBM-type swing arm assembly. The head provides up to 1.6M bytes (unformatted) of storage on a single diskette and features tunnel erase. Units are available unmounted or mounted and aligned in an OEM cartridge. Two R/W heads can be loaded simultaneously on both sides of the disc. **Tandon Magnetics Corp.**, 20731 Prairie St, Chatsworth, CA 91311. Circle 240 on Inquiry Card

HIGH RESOLUTION CRT TERMINAL

To present 100-line/in (39/cm) displays of std 8.5 x 11" (21.6 x 27.9-cm) page formats, terminal uses 15" (38-cm) diag CRT with its long axis vertical, and refreshes its display from a built-in semiconductor memory in raster scan fashion. Consisting of a 908 x 1152 dot matrix, image can be placed under full control of a host processor. All dots, simultaneously visible, are stored in dynamic RAM. Unlimited cursor capability is provided through an additional 64k bits of RAM. **Datacopy Corp.**, 3408 Hillview Ave, Palo Alto, CA 94304. Circle 241 on Inquiry Card

See us at MIDCON '77—Booth 320

CIRCLE 110 ON INQUIRY CARD



THE GREAT 4K STATIC RAM RACE

In a world of claims and counter-claims, one thing is clear. EMM SEMI is still in the lead. Of course, we not only had a healthy head start, but we field a whole family of 4K static RAMs.

We **delivered** the industry's first 4K static RAM in 1975, a full year and a half before anyone else. We are now delivering 5 basic static

RAM types with many versions of each, and producing them at an increasing annual rate of better than 3 million units in 1977, with 1978 going higher.

By now we've produced more of more different 4K static RAMs, and sold them to more customers for more different applications than anyone else in the field.

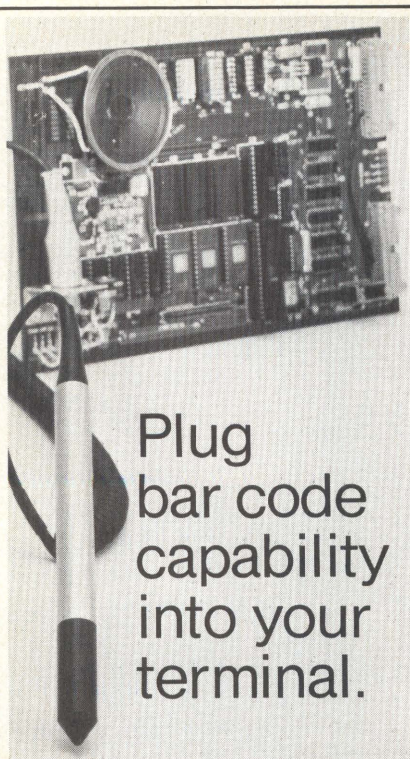
Whatever your application, from mass storage to telecommunications, from medical electronics to toys and games, chances are there's an EMM SEMI static RAM just right for you. Please call or write today for full details — and ask about our byte oriented RAMs, too.

Memory at work **EMM SEMI, Inc.**

a subsidiary of Electronic Memories & Magnetics Corporation • 3883 N. 28th Avenue, Phoenix, Arizona 85107 • (602) 263-0202

CIRCLE 111 ON INQUIRY CARD

187



Plug
bar code
capability
into your
terminal.



Save engineering time and expense. Take advantage of Intermec's years of expertise. The Intermec Model 9200 is a completely designed bar code reader that's ready to integrate into your system. All the programming needed is on the card. Read the code of your choice; Code 39, Codabar, UPC or another popular bar code. The reliable RUBY WAND® Light Pen is included in the low, low price of under \$400 in OEM quantities.

Features you'll get include bi-directional scanning, ASCII code transmission, and RS-232-C interface with dual connectors for operation with other devices. Parallel data interface boards and custom communications protocol are available or can be developed to meet your exact requirements.

For more information, write or call: Interface Mechanisms, Inc. 5503-232nd St. S.W. Mountlake Terrace, WA 98043 Phone (206) 774-3511

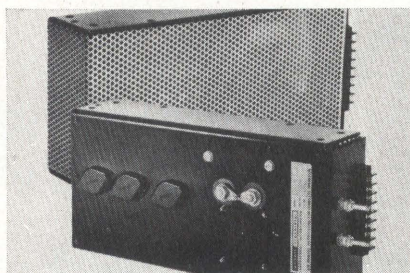
INTERMEC®

PRODUCTS

µC-BASED VIDEO TERMINAL BOARD

SCT 100 features ASCII and Baudot serial interfaces, full X-Y cursor control, screen clear, clear-to-end of line, page mode and autoscroll, 96 display char, 16-line by 64-char display, and multiple baud rates up to 300 baud ASCII. In S-100 systems, unit is powered from unregulated 7-Vdc bus; for standalone use, onboard rectifier and filter permit operation of board directly from external 6.3-Vac, 1.0-A transformer. **Vec-tron**, PO Box 20887, Dallas, TX 75220. Circle 242 on Inquiry Card

SWITCHING REGULATED POWER MODULES



Designed for telecommunications and interconnect applications, DC100 series has input power of 41 to 52 Vdc. Three units are available with outputs of 5, ± 12 , and ± 15 Vdc with total power of 100 W. Full power is available at amb temp of 55°C with 50% derating at 71°C. Line and load regulation is $>0.5\%$; pk-pk ripple is >100 mV. Measuring 5.5 x 10.5 x 2.5" (13.97 x 26.67 x 6.35 cm), modules feature overvoltage and short-circuit protection, over temp shut-down, and remote error sensing. **Abbott Transistor Laboratories, Inc.**, 5200 W Jefferson Blvd, Los Angeles, CA 90016.

Circle 243 on Inquiry Card

LINE PRINTER CONTROLLERS

Transparent to host computer diagnostics, drivers, and operating systems, plug-in modules for DEC PDP-11 and -8, Data General Nova, Interdata, and H-P 21MX computers interface to DEC LA180, Centronics, Data Printer, Data-products, Data 100, and other widely used printers. Each controller is a single PC board requiring one chassis slot and is complete with 15' (4.6-m) connecting cable. A long line parallel operation option is available to permit full speed operation up to 3000 ft (0.9 km). **MDB Systems, Inc.**, 1995 N Batavia St, Orange, CA 92665. Circle 244 on Inquiry Card

LABORATORY COMPUTER SYSTEM

Based on the LSI-11 microcomputer, TP-50 provides a range of capabilities in pulse height analysis, instrument control, and computation applications. Features include flicker-free display, push-button control panel, alphanumeric keyboard and numeric keypad, mini-floppy disc unit for data storage, and optional 40-col impact printer. The system is integrated into a cabinet including six NIM slots and 16 g-p A-D I/O slots. Option of adding std LSI-11 or PDP-11 compatible peripherals is available. **Tennecomp Systems, Inc.**, 785 Oak Ridge Tpk, Oak Ridge, TN 37830. Circle 245 on Inquiry Card

MINIATURE PCB TERMINALS

Three terminal blocks designed for external connection to PC boards are miniaturized screw/clamp types with a connecting pin that provides direct contact with incoming wire. UL recognized MK 8, AGS, and GS series offer different numbers of connecting pins and spacings for a range of working voltages. For high density wiring, the GSD 5/8 provides PCB pins at 0.1" (0.25-cm) centers. **Weidmuller Terminations, Inc.**, 4326 Eubank Rd, Richmond, VA 23231. Circle 246 on Inquiry Card

HARDWARE BOOTSTRAP FOR DISKETTE SYSTEM

Bootstrap capability for the model 210 allows a PDP-11 or LSI-11 user to load RT-11 from the diskette unit with a single command. Bootstrap instruction sequence is contained on a p-ROM which is part of the interface, saving cost and backplane slot for LSI-11 users and reducing startup time on the PDP-11. The diskette system requires no special software drivers to operate under RT-11, RSX-11, or OS/8 operating systems. **Data Systems Design, Inc.**, 3130 Coronado Dr, Santa Clara, CA 95051.

Circle 247 on Inquiry Card

WIREWRAPPING WIRE

AWG 30 25-mm wirewrapping wire is available on compact, 50' (15-m) rolls. The wire is silver plated OFHC copper with Kynar insulation. Available in four colors—red, white, blue, and yellow—insulation combines electrical and mechanical characteristics with easy stripability. It is packaged on 1.625-in (40-mm) dia spools for easy handling and storage. **OK Machine and Tool Corp.**, 3455 Conner St, Bronx, NY 10475. Circle 248 on Inquiry Card

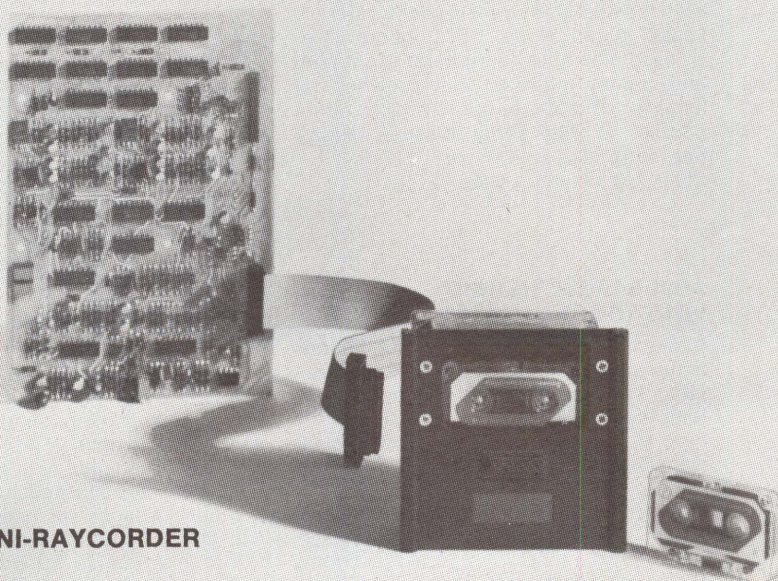
One of the Finest New OEM Products For the Computer Industry . . .

now even better

Though it looks the same on the outside, today's Mini-Raycorder incorporates many improvements which make it even more reliable, easier to use and better performing than the original design. The Model 6409 Mini-Raycorder, which scored such a resounding success as the world's first tape recorder for ANSI proposed standard Mini-Data Cassettes, is now impossible to beat.

Check these new features for yourself:

- Ball-bearing motor for improved reliability
- New servo design for better tape handling
- Full bi-directional operation available
- Optional connector configurations available for easy interfacing
- Improved cassette insertion and removal



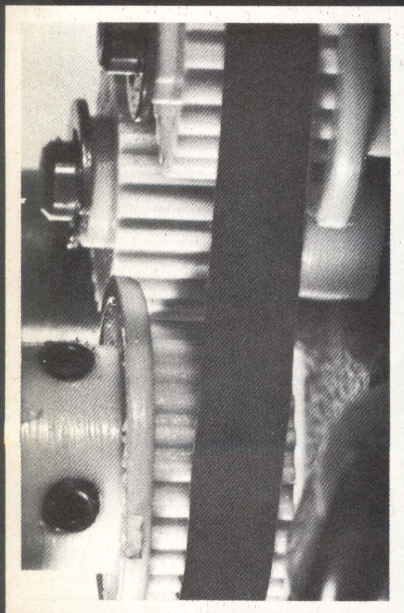
THE MINI-RAYCORDER

CIRCLE 113 ON INQUIRY CARD



Raycorder Products Division **RAYMOND ENGINEERING INC.**, 217 Smith Street, Middletown, Connecticut 06457
a subsidiary of Raymond Precision Industries

It's What's Inside That Counts



Fenner



"40 DP" TIMING BELTS

Recommended for light duty fractional horsepower applications Fenner "40 DP" timing belts offer the ultimate in synchronized engagement and precision performance. These belts have excellent flex as well as resistance to abrasion, ozone and oil. The slip-proof feature provides continuous accuracy and reduces strain on bearings as compared to flat belts or V-belts. Constant pulley gear contact insures smooth drive and minimum wear.



FENNER AMERICA
400 East Main St.
Middletown,
Conn. 06457
Tel: 203-346-7721

PRODUCTS

METAL FILM PRECISION RESISTOR

Designated type FM, metal film resistors are rated at 0.25 W at 70°C and 0.1 W at 125°C. Tolerance selections of ± 1 , 0.5, 0.25, 0.1, and 0.05% and tempco of resistance availabilities of ± 25 , ± 15 , ± 10 ppm/°C are offered. Body is molded to 0.281" (7.14 mm) max length and 0.098" (2.49 mm) max dia. Nom resistance range is 20 to 357 k Ω in std EIA, MIL, and IEC (E96, E192) values. Device is approved to MIL-R-10509F, style RN55, characteristic E, with resistance values 49.9 to 100 k Ω , all tolerances. **Allen-Bradley Co, Electronics Div**, 1201 S Second St, Milwaukee, WI 53204.

Circle 249 on Inquiry Card

CRT TERMINALS



Both 1510 editing terminal and 1520 multiprocessor terminal system feature a 1920-char display format with 24 x 80 display on 12" (30.48-cm) screen; 7 x 10 dot matrix, u/lc; generation of 128 ASCII char; refresh rate of 60 fields/s, 264 raster lines; and eight switch-selectable transmission rates to 19,200 baud. Model 1520 incorporates a programmable peripheral controller and printer interface that provides for local or remote operation with either parallel or EIA serial devices. **Hazeltine Corp**, Greenlawn, NY 11740.

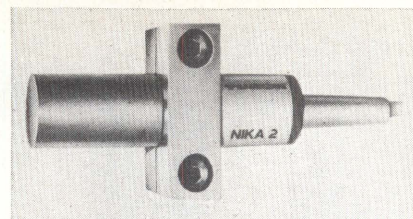
Circle 250 on Inquiry Card

ADJUSTABLE HYBRID VOLTAGE REGULATOR

Sanken SI-3580M is an output voltage adjustable regulator consisting of monolithic IC and power transistor chip. It features 1.5-A output; output current can be increased with external pass transistors. Current limiting is built into the unit which is housed in a 5-pin modified TO-3 package. Specs include input of 45 Vdc, -20 to 80°C op temp, and -30 to 125°C storage temp. **Energy Electronic Products Corp**, 6060 Manchester Ave, Los Angeles, CA 90045.

Circle 251 on Inquiry Card

PROXIMITY SENSORS AND SWITCHES



All six, low cost, inductive proximity sensors and switches of the "Economy Line" are 11 mm in diameter. They are completely encapsulated in tubular plastic housings and include removable mounting brackets. Switching ranges are 2 or 5 mm; 2-mm units may be flush-mounted in metal. Analog sensors are functional from 5 to 24 Vdc. Switches are available in 12 or 24 Vdc with normally open npn outputs as standard, or with normally open pnp, custom built. **Turck Multiprox, Inc**, 9710 10th Ave N, Minneapolis, MN 55441.

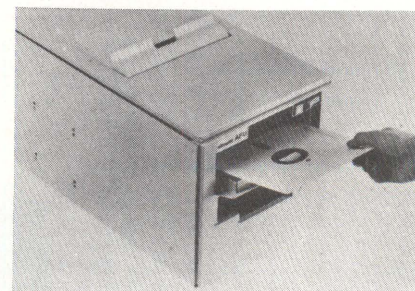
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TEMPERATURE COMPENSATED CRYSTAL OSCILLATORS

TCXO 2211 and 2200 are designed to operate in the 4- to 20-MHz range. Precision crystals and computer-selected compensating elements provide a std frequency stability of ± 1 ppm over an op temp range of -40 to 70°C (2211 series) and 0 to 55°C (2200). Both are compatible with TTL loading and provide a frequency trim control for precise adjustment. Series 2211, hermetically sealed, requires 12 Vdc at 15 mA. 2200, in an epoxy-molded package, operates from 5 Vdc. **Dale Electronics, Frequency Control Group**, 930 W 23rd St, Tempe, AZ 85282.

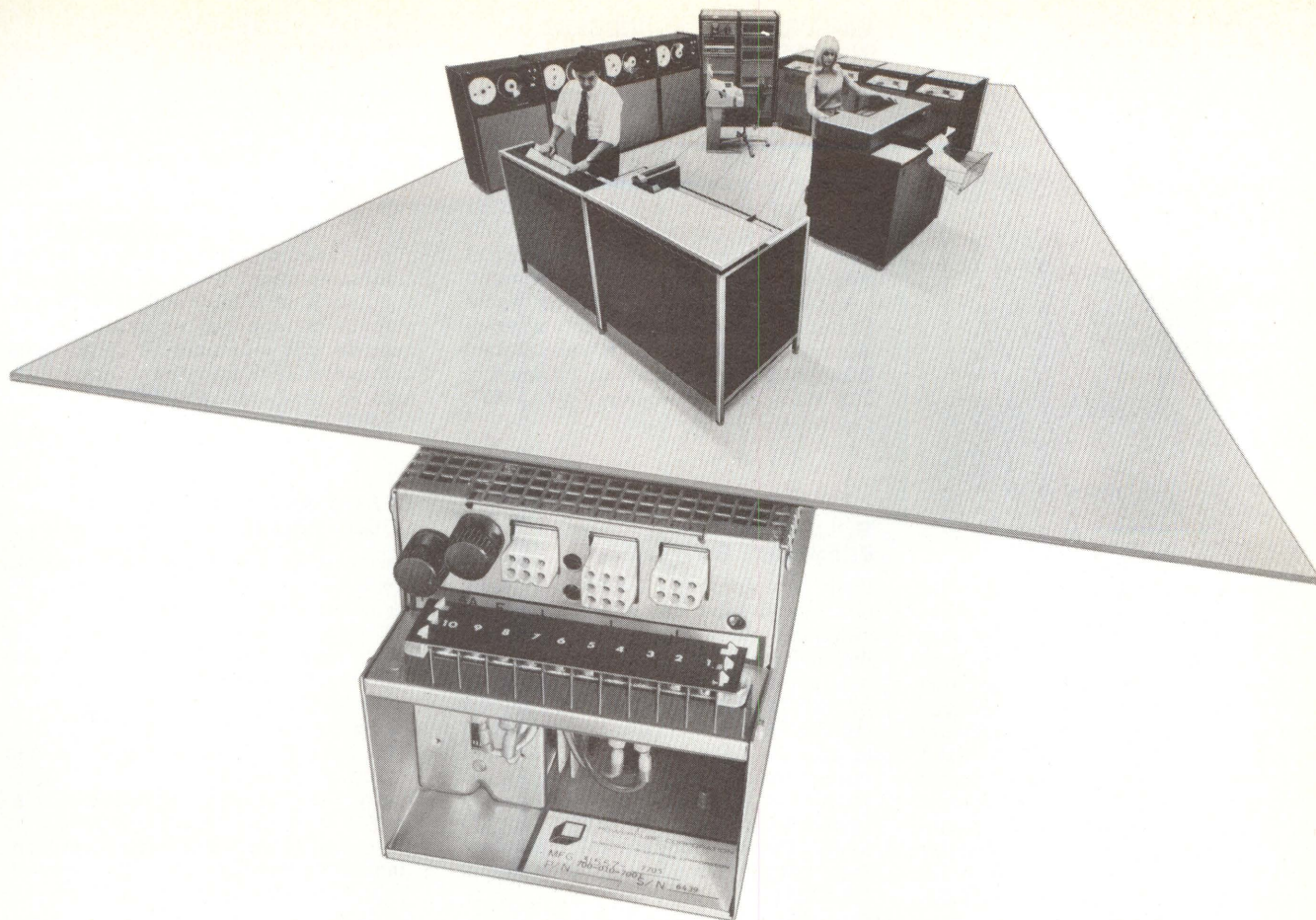
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AUTOMATIC FLOPPY DISC UNIT



Compatible with IBM 3740, automatic floppy disc unit consists of an automatic loader, two interchangeable floppy disc drives with dual read/write heads, and a power supply unit. Max capacity is 20 diskettes stacked one on top of the other. Length of automatic loading cycle is approx 5.5 s. A separate feed slot is available for manually changing diskettes. **Olivetti Corp of America**, 500 Park Ave, New York, NY 10022.

Circle 254 on Inquiry Card



Powercube's new off-line switcher will hold you up for 50 milliseconds

Minicomputers, modems, microprocessor-based systems, multiplexers — whatever your application, you want reliability in your off-line switching power supply.

Powercube provides it.

Our new OLS Model 10 175-watt multiple-output series is designed for nominal input voltage of 115/230 VAC, 43 to 63 Hz. But it tolerates wide dynamic input fluctuations to assure continuous operation during "brown-out" conditions.

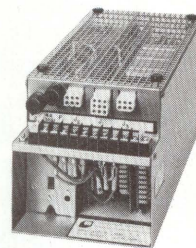
What's more, typical hold-up of output voltages is 50 ms at full load and nominal input, providing the longest possible housekeeping in anticipation of power failure.

And, there's more you'll like.

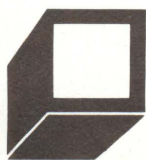
Borrowing on years of space-age power supply technology, Powercube has packaged this powerful unit in a compact, $5\frac{1}{2}'' \times 5\frac{1}{2}'' \times 11''$ envelope. You can use it almost anywhere. The OLS Model 10 is also 90% modular — a real time-saver when it comes to maintenance.

You get valuable extra features, too — features that are extra cost options in other units. Like a "drop-out" signal that indicates input AC power status. And an input line filter that meets VDE and other domestic and international requirements.

Get the full story. Circle the reader response number or phone 617-891-1830.



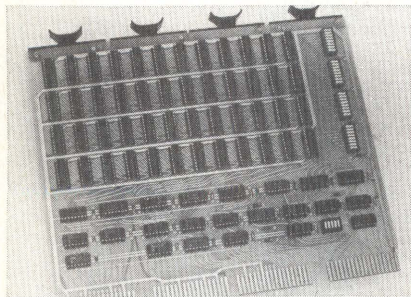
Big power in a small package: +5 V @ up to 24 A; ± 12 V @ up to 4 A each; ± 15 V @ up to 4 A optional.



POWERCUBE® CORPORATION
214 CALVARY STREET, WALTHAM, MASS. 02154 (617) 891-1830
SUBSIDIARY OF UNITRODE CORPORATION

PRODUCTS

PDP-8 COMPATIBLE 16k STATIC RAM



Available in 4k x 12, 8k x 12, 12k x 12, and 16k x 12 models, the VM816 semiconductor memory system is completely hardware and software compatible with std PDP-8 operating systems. It plugs directly into the OMNIBUS[®] chassis, offering up to 16k words of memory per slot. The 4096 x 1 n-MOS static RAM design utilizes 31 A at 5 Vdc for every 16k capacity. Four field-select DIP switches allow easy field assignment for each 4k increment. **Computer Extension Systems, Inc.**, 17311 El Camino Real, #176, Houston, TX 77058. Circle 255 on Inquiry Card

MINIATURE INCANDESCENT INDICATOR LIGHTS

For use at 2 to 120 V, indicator lights mount in 0.6875" (1.745-cm) mounting holes and are intended for use with T-3¼ miniature bayonet-base incandescent lamps. Lights are UL and CSA listed and meet or exceed MIL-L-3661 requirements. Lenses may have stove-pipe, dome, convex, flat, or cylindrical shapes; finish options are transparent, translucent, internally-fluted, back-frosted, and matte-black. Both screw-in and screw-on lens holders are available. **Dialight, a North American Philips Co.**, 203 Harrison Pl, Brooklyn, NY 11237. Circle 256 on Inquiry Card

SOLID-STATE PRESSURE SWITCHES

Each weatherproof (NEMA 4) series 604 switch uses Hall effect solid-state switching element in conjunction with the company's dual-snap negative rate disc spring which has amb temp range of -30 to 160°F (-1 to 71°C). Single circuits regulate input voltage of 6 to 16 Vdc down to 6 to 10 mA input current max. Max output is 8 to 20 mA. Models are available in pressure ranges from 0.8 to 4700 lb/in² (5.52 to 32,430 kPa). **Custom Component Switches, Inc.**, 21111 Plummer St, Chatsworth, CA 91311. Circle 257 on Inquiry Card

DATA ACQUISITION METER INDICATOR

Model RS is designed to interface with pressure transducers and load cells to provide a precise measuring system for data acquisition and control applications. Each 4.5 x 6.75" (11.43 x 17.14-cm) unit contains basics of company's series 100 signal conditioner plus a digital readout, transducer excitation, zero/span adjustments, and signal amplifications of 0 to 1 and 1 to 10 Vdc output. Interconnections are made by user through rear-mounted 30-pin edge connector. **Tyco Instrument Div.**, 4 Hartwell Pl, Lexington, MA 02173. Circle 258 on Inquiry Card

STATIC AND DYNAMIC LOGIC PROBE

Designed to test static and dynamic conditions in digital circuits, the self-contained LP-2 measures 5.8 x 1.0 x 0.7" (14.7 x 2.5 x 1.8 cm). Drawing power from the circuit under test, probe provides pulse detection of 300 ns and pulse stretching functions at a rate of 10 Hz for instant readout of TTL, DTL, HTL, and CMOS levels, positive and negative transitions, and pulse symmetry. Device offers measurement within 0.15 V of logic levels and transitions with positive go/no-go indication. **Continental Specialties Corp.**, 44 Kendall St, New Haven, CT 06509. Circle 259 on Inquiry Card

Introducing the first keyboard with seals that protect it from inhuman conditions. And humans.



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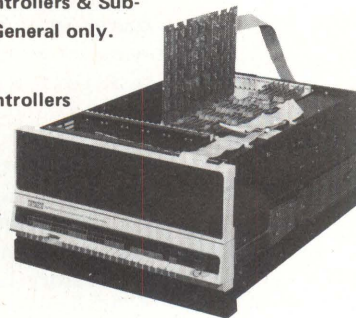
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The Training

With the advent of the microprocessor, your design team now faces a new kind of development process, a process which brings with it an unprecedented opportunity for design flexibility. It also brings a process where proper training on the equipment and hardware/software integration techniques are of vital importance.

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The Service

In the unlikely event that repairs should be necessary on the development system, Leasametric will initiate either in-house service or a replacement system within 24 hours—at no additional cost.

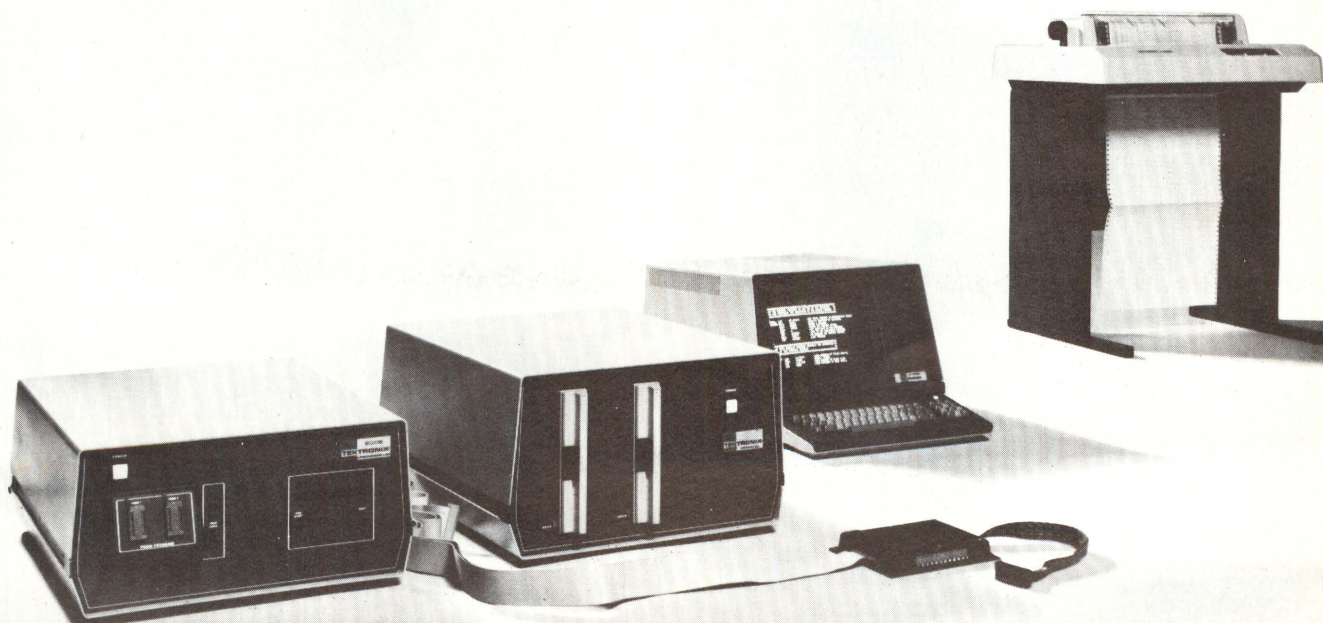
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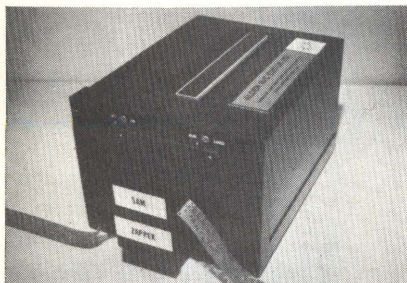
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PRODUCTS

NC PROGRAM LOADER PUNCHED TAPE



Zapper is a small, high speed reader which loads NC punched tape programs into company's standalone memory (SAM). Unit reads and transfers parts of program data at speeds up to 300 char/s into solid-state memory storage. It also loads programs into company's stored program tape editor for use in preparing, duplicating, and editing NC parts programs. Reader measures 6.5 x 8.25 x 11" (16.51 x 20.95 x 27.94 cm) and weighs 13 lb (5.85 kg). **Alden Self-Transit Systems Corp.**, NC Editor Div, 2 Mercer Rd, Natick, MA 01760. Circle 260 on Inquiry Card

PDP-11-COMPATIBLE MAG TAPE SYSTEM

Introduced for the DEC PDP-11 mini-computer, the T9000 mag tape memory system incorporates a 75-in (190.5-cm)/s tape transport. Complete PDP-11 system integration is possible without software changes. The 9-track controller is available in an 800-bit/in (315/cm) NRZI version or both NRZI and 1600-bit/in (630/cm) phase-encoded formats. It runs RSX-11, RT-11, and DOS unaltered, and is TM11/TU10-compatible on all commands and status vector interrupts. **Computer Labs, Inc.**, 505 Edwardia Dr, Greensboro, NC 27409. Circle 261 on Inquiry Card

BOUNCE FREE LIMIT SWITCH

Built around the rugged LC2 mercury film switch, the LC2P-1839 limit switch is encapsulated with a tested MTBF of >2G cycles. This welded steel capsule has one moving part—a flexing armature spring which carries a film of mercury to merge with a similarly wetted stationary contact. Mercury film contacts provide a contact resistance of 0.2 Ω measured at microampere levels or at power loads to 2.0 A. Resistance changes by <0.015 Ω over switch lifetime. NO or NC contacts are available. **Fifth Dimension Inc.**, 707 Alexander Rd, Princeton, NJ 08540. Circle 262 on Inquiry Card

1250- AND 1500-LINE/MIN PRINTERS

DOC 1250 and 1500 line printer subsystems, with integrated microprocessor controller, are fully buffered 132-char units with single spacing. Plug compatible with the 1403, the printers have a power driven forms stacker and cover. Std features include increased throughput, 6-part form printing, interchangeable print bands utilizing a universal char set buffer, forms spacing through a forms control buffer, vertical line spacing at 6 or 8 lines/in (2.4 or 3.14/cm), and a slew rate of up to 75 in (191 cm)/s. **Documation Inc.**, PO Box 1240, Melbourne, FL 32901. Circle 263 on Inquiry Card

0.5" LED DIGITS

DL-520 digits are available in 1-, 1½-, and 2-digit DIPs as well as in 2- to 6-digit modules with PCB edge connectors; the 1½-digit DIP has a polarity indicator. All displays operate off a 5-V TTL supply, feature a decimal point after each digit, have common anode or common cathode terminals, and are available with a red or clear plastic cap. Digits packaged in DIPs may be butted end-to-end to create displays of any length with equal spacing between digits. **Litronix Inc.**, 19000 Homestead Rd, Cupertino, CA 95014. Circle 264 on Inquiry Card

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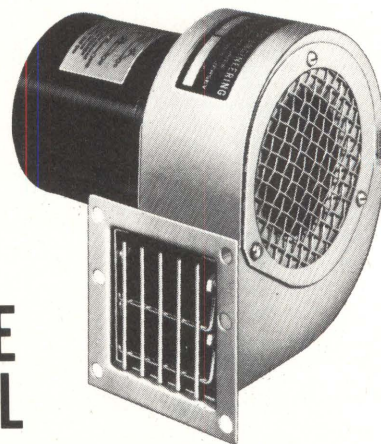
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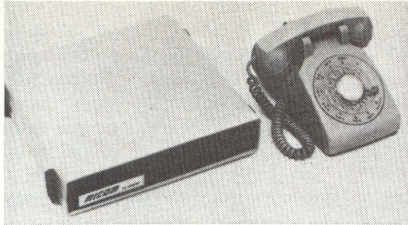
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REMOTE DATA ENTRY TERMINALS



A family of data entry terminals which interface with the company's Link 100, 200, or 500 computers enable remote sites to use the central computer without a leased line. Data are stored on a flexible disc; the remote site confers with the computer as necessary. Devices offer send/receive batch capability and file capacity of 311,168 char, organized as 2431 addressable lines of 128 char each. Avg access time is 0.3 s. **Randal Data Systems, Inc.**, 365 Maple Ave, Torrance, CA 90503.

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OUTER ROTOR BRUSHLESS DC MOTORS

A line of brushless dc motors for critical speed applications, the DCB series has a 3-phase ac motor with a drive and control circuit coupled with the outer rotor's flywheel effect to provide high inertia. Brushless design eliminates electrical commutation noises. Units can run at synchronous speeds at any setting, maintaining preset speed despite changes in line voltage or frequency. Std motors have 12- or 24-V inputs with different speed and torque outputs. **Nidec America Corp.**, 1821 University Ave, St Paul, MN 55104.

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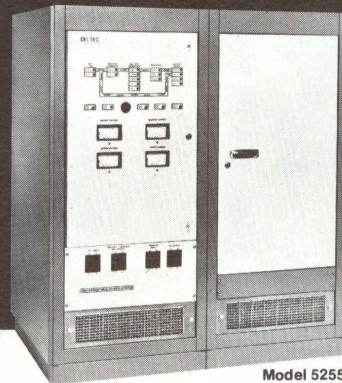
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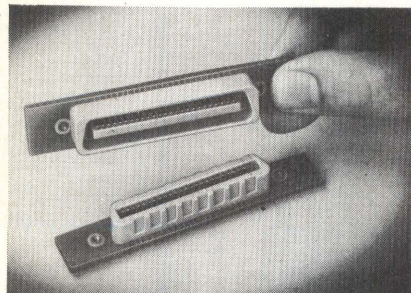
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PRODUCTS

PC BACKPLANE I/O CONNECTORS



A Tel-Com connector series for telecommunications and computer systems circuitry mates with similar telephone cable I/O connectors. Contacts are pressfit into plated-through holes creating solderless gas-tight connections. Insulator housings are pressfit onto contacts, preloading cantilever beams and creating a closed entry type connector. Dual 25 and 32 positions on std 0.085" (0.216-cm) centers are available in male and female styles. **Methode Electronics, Inc., Connector Div., 7447 W Wilson Ave, Chicago, IL 60656.** Circle 268 on Inquiry Card

ROM SIMULATOR RS-232-C INTERFACE

RS-232-C interface plugs into SMS ROM simulator mainframe, allowing direct connection to host computer and eliminating paper tape handling errors and tape punch hardware. Reflected data are provided to user for software verification of transmitted data. Use of same data/control format as paper tape reader allows existing software to be utilized with output driver modification. Load times for 1k x 4-bit and 1k x 8-bit memory modules are 40 and 50 s with 50-char/s readers and 17 and 25 s for 120-char/s readers. **Analytix Electronic Systems, Inc., 106 Daniel Webster Hwy, Nashua, NH 03060.** Circle 269 on Inquiry Card

300-LINE/MIN OCR PRINTER

Directed to retail organizations, the 300-line/min OCR printer generates both general merchandise labels and end-of-day inventory and accounting reports with a simple ribbon change, eliminating the need for two printers. High performance model is available with 132-col print widths, using pin-feed tractors and continuous fan-fold paper up to 7.5" (19 cm) wide. Parallel interface is std; an RS-232-C interface is optional. **Data 100 Corp., 6110 Blue Circle Dr, Minneapolis, MN 55435.** Circle 270 on Inquiry Card

ELECTRONIC ASSEMBLY TEST EQUIPMENT

An advanced version of the system 331 computer-controlled functional tester features multifunction digital display, UUT serial number entry, pre-wired analog chassis, and control and peripheral chassis as std. Expansion is possible by plugging in selected modules. Offered options include dual floppy disc system, autocal with removable stds, and IEEE bus port with supporting software. **SIR-Atlanta, Inc., 331 Luckie St, NW, Atlanta, GA 30313.** Circle 271 on Inquiry Card

DATA ACQUISITION CASSETTE READER

633M series tape cassette modules are designed for remote use with 12-V power sources. Scanning rates of up to 32 samples/s are achieved using 8-phase driver coupled to a high resolution stepping motor. Storage capacity is >10M bits on std Philips-type 300' (66.2-m) digital cassettes. 633M/8 records 1.2M bytes at 150 bytes/s and features DMA mode recording for high performance with 8-bit microprocessors. 633M/12 records 0.8M words at 100 words/s. Model 12A reader is available for either unit. **Sea Data Corp., Winfield Hill, 153 California St, Newton, MA 02158.** Circle 272 on Inquiry Card

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MODEL 612



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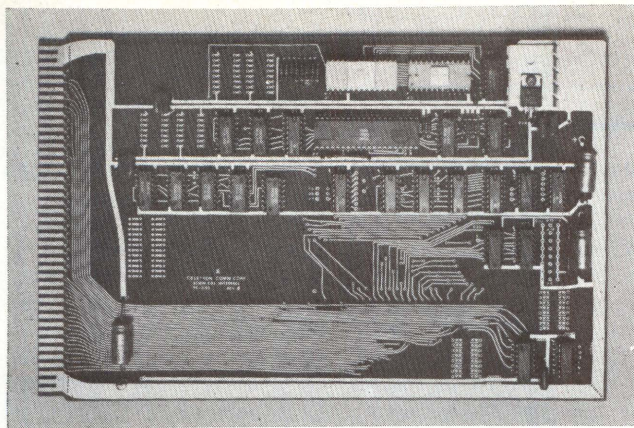
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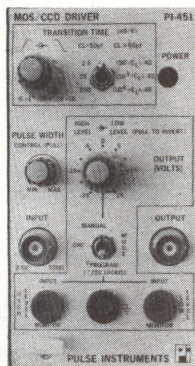


Utilizing hardware for mathematical calculations, board interfaces MOS Technology 7529-103 calculator chip to 8080, Z80, 6800, and other microprocessor systems. Basic and complex math functions can be done with simple software and a min of system memory. Calculations involving interpreters or compilers that would require 8k to 16k of memory can be done in less than 1k. Functions include trig, inverse trig, logs, antilogs, exponentiation, and factorials; two parentheses levels are supported. The board can be used to supplement the functions of a small interpreter, as a standalone firmware math package, or programmed to emulate the functions of a programmable calculator. **Mini Micro Mart**, 1618 James St, Syracuse, NY 13204.
Circle 273 on Inquiry Card

MODULAR LOAD CELL SIGNAL CONDITIONER

Model 166 Bridgesensor, a complete bridge instrumentation "system" in a 2 x 2 x 0.6" (5 x 5 x 1.5-cm) module, allows output to be fed directly into a microprocessor or digital display. It contains an adjustable bridge power supply, differential instrumentation amp, V-F converter, and optically isolated output stage. An external ± 15 -V power supply and load cell complete the weighing system. Bridge supply is adjustable from 4 to 10 V and can supply up to 100 mA. Differential amp has adjustable gain from 10 to 1000 and an input impedance of 10 M Ω . Input stability of the amp is $> \pm 0.5 \mu\text{V}/^\circ\text{C}$; output is ± 10 V at 5 mA. **Calex Manufacturing Co, Inc**, 3305 Vincent Rd, Pleasant Hill, CA 94523.
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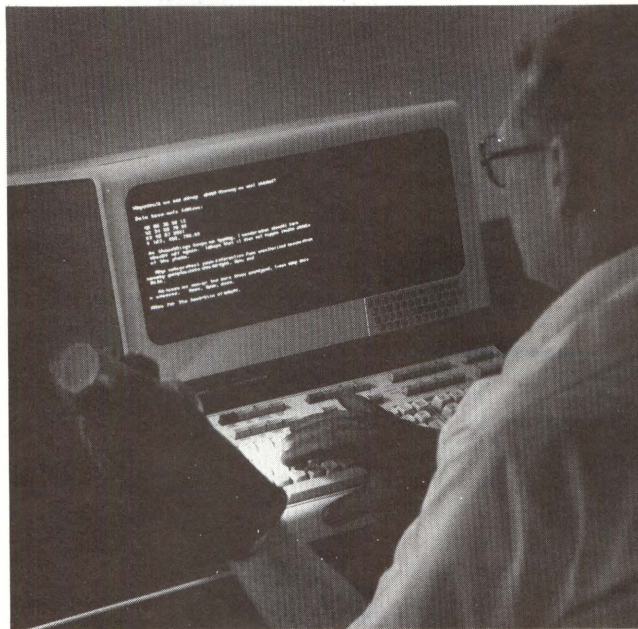
TM-500 PLUG-IN UNIT



The plug-in PI-451 programmable MOS/CCD driver is designed to operate in Tektronix TM-500 series power mainframes. Primarily a level shifter which converts a TTL input signal into a ± 25 -V output signal, it is well suited for driving most MOS-type devices and other capacitive loads. Output high and low levels are independently adjustable. In manual mode, they are varied by front panel controls. In voltage programmable mode, they are controlled by input voltage levels connected to front panel input jacks. Digital programming is available as an option. Output transition times are variable from < 2.5 ns/V to $> 2.5 \mu\text{s}/\text{V}$. **Pulse Instruments Co**, PO Box 1655, San Pedro, CA 90733.

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Computer-information thieves are among the most sophisticated of all white-collar criminals. Data transmission, processing, and storage are all open to the potential threat. Whether you are using small, medium, or large-scale computers or shared-resource networks.

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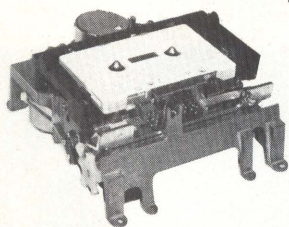
If you're interested in making your computer data electronically safe, you need copies of the free booklets, "Computer Threats" and "The Info-guard Security Kit." Then we can talk about hardware prices and delivery. Call James Booth, 602/949-4111 or write to him at Motorola Government Electronics Division, Dept. F-2, P.O. Box 2606, Scottsdale, AZ 85252.



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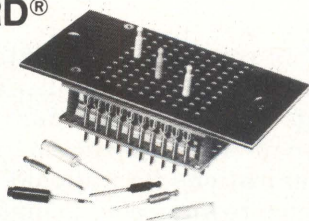
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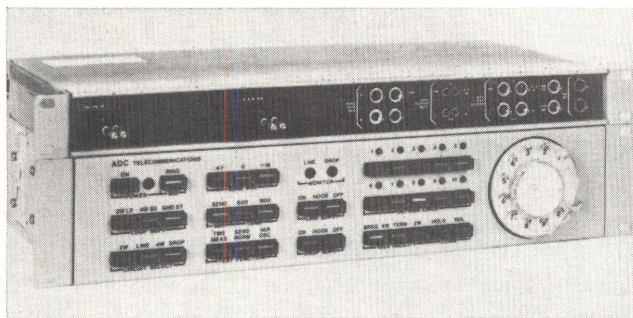
PRODUCTS

50-MHZ SWEEP/FUNCTION GENERATOR

Model 757 contains two generators in one package. The main generator produces sine, triangle, and square waveforms at any frequency from 0.0001 Hz to 50 MHz; the ramp/step generator produces ramp and step waveforms with periods ranging from 1 μ s to 1000 s. Main generator can free run or be triggered or gated manually, externally, or internally by the ramp/step generator. Internally triggered, it causes the unit to generate positive or negative pulses as narrow as 10 ns, having rise and fall times of <5 ns and peak amplitudes up to ± 7.5 V into 50 Ω . Ramp/step generator can free run or be triggered or gated manually or externally to produce a waveform with 11 levels. LEDs indicate which of the 11 levels is at the output. **Exact Electronics Inc.**, 455 SE 2nd Ave, Hillsboro, OR 97123.

Circle 276 on Inquiry Card

PRIVATE LINE TEST UNIT



Composed of an access panel and a test panel, which together require only 5.25" (13.34 cm) of rack space, the Carrier Maintenance Test Facility mounts in a carrier bay or wherever private-line and toll circuit testing is required. Circuit access is furnished by jacks and cord reels in the access panel; test panel provides test control and supervision, including 2-wire loop, 4-wire simplex, and ground start. Ten keyset telephone lines provide communication. In addition, the facility under test can be used as a talk path on either a bridged or terminated basis. Signaling is via a rotary dial mounted in the panel. External test equipment may be connected to provide additional capability. **ADC Telecommunications**, 4900 W 78th St, Minneapolis, MN 55435. Circle 277 on Inquiry Card

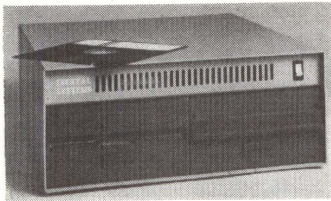
ALPHANUMERIC DISPLAYS FOR MULTIPLEX CIRCUITS

Pinlite MDD-63, -64, and -65 incorporate required isolation diodes directly within the case of the unit, simplifying use of efficient multiplex circuits in telecommunications and avionics systems, microprocessors, and data acquisition and measurement equipment. The 0.765 x 0.375 x 0.900" (1.943 x 0.953 x 2.057-mm) packages save behind-panel space and simplify overall circuit design. Each display features patented corner crossover which allows full characters with no corner gaps. MDD-6 series displays are available in 3-, 4-, or 5-V configurations with up to 9000-ft-L brightness; each 0.3125" (7.937-mm) alphanumeric character is life rated at 100 kh/segment avg. **Refac Electronics Corp.**, PO Box 809, Winsted, CT 06098.

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DOUBLE-DENSITY FLOPPY DISC SYSTEM

Recording density is hardware and/or software selectable on the FDC-3 controller board. Users may choose either IBM 3740 format or a double-density format of 571k bytes/diskette (77 tracks of 58 sectors with 128 bytes/sector). Avail-



able separately or in 8080 systems consisting of up to eight Shugart disc drives, controller board operates with CP/M software, a complete disc operating system including a text editor, assembler, and dynamic debugging tool. Write protect option can be hardware enabled or selected with notched diskettes. Other features include DMA, hardware bootstrap loader, CRC error check, and Z80 compatibility. An S-100 interface card is included. **Digital Systems**, 6017 Margarido Dr, Oakland, CA 94618.

Circle 279 on Inquiry Card

SERIES/1 COMPATIBLE SOFTWARE PACKAGE

Allowing a Series/1 processor to communicate with remote systems in a mode compatible with IBM's binary synchronous communications protocol, the 3270 BSC package supports point-to-point and multipoint communications and provides a terminal display option for supporting clustered terminal configurations using either IBM display stations or TTY-compatible CRTs. Fully compatible with existing IBM 360/370 BSC communications software, the package can be used as a direct replacement for 3270 systems. Min hardware requirements consist of processor, 32k main storage, BSC single-line control feature, and display stations such as IBM 4979 or 4978, or TTY-compatible hardware. **Conversational Systems Corp**, 31 E 28 St, New York, NY 10016.

Circle 280 on Inquiry Card

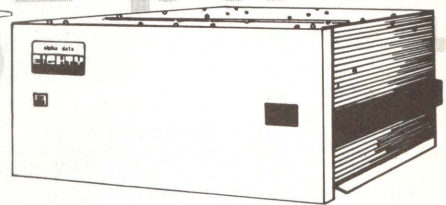
µP-CONTROLLED TRANSACTION RECORDER



System 80, designed for data acquisition and data logging applications, features a cassette recorder and 8080 microprocessor controller. Optional input devices include an integral, 17-char badge reader and 32-key calculator style keyboard with 9-digit display. Keyboard legends may be customized using removable overlays. An external device interface permits attachment of a bar code scanning light pen, A-D converter, or external event sensors. All input data are received by the 8080 controller, permitting processing and sequence/error checking before recording on tape. The microprocessor allows the system to be programmed and tailored for specific data entry and data acquisition situations. Tape capacity is greater than 125k bytes. **Danyl Corp**, 310 Cooper Ctr, N Park Dr and Browning Rd, Pennsauken, NJ 08109.

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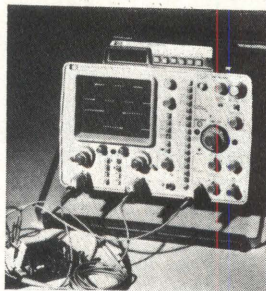
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Measuring the time between two observed events with 1% accuracy, model 1725A has built-in dual-channel, delta time capability. An optional 3½-digit autoranging digital multimeter reads time in seconds, milliseconds, or microseconds. In delta time mode, the instrument measures time between two events on either channel A or B, or between one event on each channel. Time intervals as short as 1 ns can be measured. An 8 x 10-cm display allows dual trace signals to be viewed accurately. Stable internal triggering to 275 MHz requires only 1 cm of vertical deflection (only 0.5 cm to 100 MHz). Triggering on line frequency can be selected. Stable external triggering requires only 50 mV pk-pk to 100 MHz. **Hewlett-Packard Co**, 1507 Page Mill Rd, Palo Alto, CA 94304.

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INTERFACE BREAKOUT PANEL



A battery powered, handheld instrument, model 80 is designed to monitor and breakout a std CCITT V.35 interface between a modem and a terminal. To use, the operator unplugs the V.35 interface cable between modem and terminal, and plugs it into the unit. This allows access to all 17 signal conductors specified by V.35 or Bell 306 interface specs. Each conductor is monitored by high impedance sensing circuits with LEDs to indicate the on or off state. Balanced data and clock signals are monitored by a balanced receiver with LED indicator. 13 switches allow all interface signals to be interrupted. Pins next to each switch allow miniature jumper cables to be used for crosspatching of signals. **International Data Sciences, Inc**, 100 Nashua St, Providence, RI 02904.

Circle 283 on Inquiry Card

PCB FIBER-OPTIC TERMINAL SETS

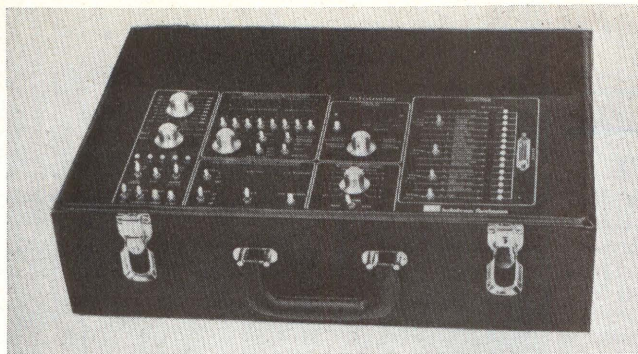
Fiber-optic transmitter and receiver terminal sets for direct mounting on closely spaced PC cards, MODAL Superdips have the fiber-optic connector perpendicular to the pins. Overall dimensions are 1 x 0.5 x 0.4" (2.5 x 1.3 x 1.0 cm)



with pin-spacing compatible with std 14-pin DIPs. There are three or five active pins for connection to power supplies and input and output functions. Available in this format are MDL421, a digital data system for transmission of TTL-compatible signals over distances up to 100 m from dc to 2M bits/s, and analog system MDL238 (dc to 50 MHz), which has the transmitter split into an LED module and driver in a separate DIP. **Meret Inc**, 1815 24th St, Santa Monica, CA 90404.

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MODEM/MULTIPLEXER TEST SET



Functions of the portable Infotester TE 600 include detection and display of bit and block error rates, determination of request to send and clear to send turnaround times, and measurement of distortions and overspeed variations. Front panel controls are arranged for step-by-step operation. Each knob and switch has only one function, eliminating the confusion caused when a switch has different functions in different modes. Indicator lights and LED display are used to display status and test results. Unit is RS-232-compatible and operates at data rates from 50 to 19,200 bits/s, analyzing performance of synchronous and asynchronous modems and frequency and time division multiplexers. **Infotron Systems Corp.**, 7300 N Crescent Blvd, Pennsauken, NJ 08110. Circle 285 on Inquiry Card

9600-BAUD PORT EXPANDER

Series 7700 consists of a cluster controller and up to 32 remote parallel I/O interfaces, providing full-duplex communication at up to 9600 baud via the RS-232 port of computer or data processor. Individually addressable remote interfaces feature an 8-bits-plus-strobe parallel I/O and polled receive and/or transmit capability, and require only a 4-wire, 20-mA current loop. Cluster controller and remote interfaces are similarly packaged, and include built-in power supply. Package size is 5.75 x 5.50 x 15" (14.6 x 13.97 x 38.10 cm). Options include current loop or TTL cluster controller input I/O, and separately addressable receive and transmit at each remote interface. **Kewau Enterprises, Inc.**, 1750 Sheffield Dr, Ypsilanti, MI 48197. Circle 286 on Inquiry Card

µP HEXADECIMAL KEYPAD ACCESSORY

For use with Mini-Micro Designer (MMD-1) training and development microcomputer, MMD/HEX-1 and -2 keypads provide a convenient method for programming with 4-bit binary



hexadecimal code. Calculator-type 16-key array with eight additional function keys permits users to execute programs, modify, or examine contents of memory and registers, and to monitor program performance. All keys are priority encoded. A factory-programmed HEX L/D p/ROM for hexadecimal conversion replaces the HEX p/ROM. One pair of 0.3" (0.76-cm) high LED hexadecimal displays is furnished with each -2 keypad; two additional pairs are optional. Both keypads are furnished with conversion p/ROM, ICs, and a 28-pin double-ended interconnection cable. **E&L Instruments, Inc.**, 61 First St, Derby, CT 06418. Circle 287 on Inquiry Card

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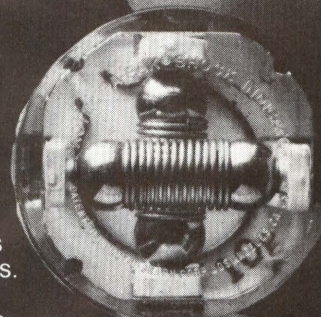
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Modular Power Supplies

Short-form catalog focusing on dc-dc converters, ac-dc miniature modules, and ac-dc high power supplies includes application design notes which give methods for decoupling loads from bus system, and grounding multiple loads. **Analogic**, Wakefield, Mass.

Circle 300 on Inquiry Card

Power Supplies

Catalog groups supplies by application requirements, presenting specs as well as thermal tables, glossary of NEMA terms, and conversion tables. **Technipower, Inc.**, Ridgefield, Conn.

Circle 301 on Inquiry Card

Distributed Data Processing

"Distributed Data Processing: The Practical Alternative" describes advantages and explains how to match resources to evolving needs to provide better control. **Digital Equipment Corp.**, Maynard, Mass.

Circle 302 on Inquiry Card

Miniature Printed Circuit Relays

Class 76 relay catalog is complete with specs, dimensional drawings, wiring diagrams, and pc layouts for single and double pole versions. **Magnecraft Electric Co.**, Chicago, Ill.

Circle 303 on Inquiry Card

Failure-Immune Computer Processing

Color photos, and hardware and software configurations illustrate folder explaining hardware and software organization for nonstop, failure-immune processing. **Tandem Computers, Inc.**, Cupertino, Calif.

Circle 304 on Inquiry Card

Add-On Memory News

Newsletter designed to keep present and potential users informed of important activities and market developments will be published on quarterly basis. **Electronic Memories and Magnetics Corp.**, Computer Products Div., Hawthorne, Calif.

Circle 305 on Inquiry Card

CMOS ICs

Technical specs, applications, charts, and diagrams pertaining to complete line of CMOS ICs are found in handbook which includes LSI technology developments. For copy send \$3 to **National Semiconductor Corp.**, Mktg Services Dept., 2900 Semiconductor Dr., Santa Clara, CA 95051.

Refresh Memory Display

Block diagram illustrating the EyeCom model 808 configuration highlights brochure which examines line of solid-state B/W and color displays. **Spatial Data Systems, Inc.**, Goleta, Calif.

Circle 306 on Inquiry Card

Network Interconnect Channel

Outlining the high speed transmission technology and systems architecture, brochure highlights user benefits, applications, and features of HYPERchannel. **Network Systems Corp.**, Brooklyn Center, Minn.

Circle 307 on Inquiry Card

Data Acquisition System

Leaflet on model 90MC1 programmable microprocessor-controlled datalogger describes components by giving key specs and features, and provides dimensional and mounting information. **Consolidated Controls Corp.**, Bethel, Conn.

Circle 308 on Inquiry Card

Power Supplies

Guide discusses the make or buy decision, addresses custom vs standard packaging problems, and explains how to specify high voltage power supplies, using oil as an insulator, and safe packaging for high voltage circuits. **AMP, Inc.**, Capatron Div., Elizabethtown, Pa.

Circle 309 on Inquiry Card

Data Sets and Couplers

Connection arrangements, station configurations, and data rates are described in fact sheet illustrating FCC-registered equipment. **General DataComm Industries, Inc.**, Wilton, Conn.

Circle 310 on Inquiry Card

Memory Test System

DR-12/40, a computer-controlled semiconductor memory test system, is depicted in brochure which furnishes specs and uses diagrams and illustrations to explain system operation. **Adar Associates, Inc.**, Burlington, Mass.

Circle 311 on Inquiry Card

Miniature Lamps

With basic information and design considerations sections, catalog covering miniature incandescent, halogen, and fluorescent lamps has drawings, data, and specs arranged according to bulb size. **General Electric Co.**, Miniature Lamp Products Dept., Cleveland, Ohio.

Circle 312 on Inquiry Card

Sockets and Connectors

Complete pricing information is available for full line of sockets, connectors, and other products found in catalog. **Optical Electronics, Inc.**, Tucson, Ariz.

Circle 313 on Inquiry Card

Circular Environmental Connectors

Catalog with cutaway/dimensional drawings and insert configurations describes three lines of miniature and high density connectors. **Amphenol North America Div.**, Bunker Ramo Corp., Oak Brook, Ill.

Circle 314 on Inquiry Card

Microelectronic Packaging Systems

Brochure covers line of microelectronic packaging systems as well as associated hardware such as cable assemblies, component carriers, frames, and enclosures. **Mupac Corp.**, Brockton, Mass.

Circle 315 on Inquiry Card

Modular Computer Systems

Booklet made up of data sheets with specs and features for 21 MX-based systems discusses memory systems, hardware and microprocessing accessories, and data communication, terminal, and instrumentation interfaces. **Hewlett-Packard Co.**, Palo Alto, Calif.

Circle 316 on Inquiry Card

Memory Interface

Specs, schematics, application notes, and function tables for sense amplifiers, MOS drivers, and memory are provided in 232-page "The Memory Interface Data Book for Design Engineers." **Texas Instruments, Inc.**, Dallas, Tex.

Circle 317 on Inquiry Card

Card Edge Connectors

Information on design and construction, specs, and dimensional drawings are supplied in technical bulletin on series CM, CE, CH, and PC connectors. **Eby Co.**, div of **REDM Corp.**, Philadelphia, Pa.

Circle 318 on Inquiry Card

Communications Glossary

Comprehensive glossary of computer communications and telecommunications terminology includes definitions used in technologies such as packet switching and fiber optics. Price is \$1. Specify French or English version. **The Computer Communications Group**, TransCanada Telephone System, 12-160 Elgin St., Ottawa, Ontario K1G 3J4, Canada.

Power Line Disturbance Monitor

Literature gives specs, options, and performance characteristics pertaining to model 3500 power line disturbance monitor. **Programmed Power Div, Franklin Electric Co, Sunnyvale, Calif.**
Circle 319 on Inquiry Card

Automatic Test Support Systems

Brochure describes the Spartan LSI/MSI system and T-1000 microcomputer, and discusses system/application software, fail-all simulator, and application test programs. **Dynamic Sciences, Inc, Sepulveda, Calif.**
Circle 320 on Inquiry Card

DIP Sockets

Catalog with specs and features covers line of solder and wrap type DIP sockets with bifurcated or collect style contacts, and lists sockets on 0.100 through 0.600" (0.254 to 1.524-cm) grids with 2- to 40-pin configurations. **Aries Electronics, Inc, Frenchtown, NJ.**
Circle 321 on Inquiry Card

Radioimmunoassay Data System

Application note on radioimmunoassay data system (RIADS) contains system description, software functions, and benefits, and displays an actual standard curve as it appears on CRT. **Wang Laboratories, Inc, Lowell, Mass.**
Circle 322 on Inquiry Card

DC Power Supplies

Outlining performance capabilities, catalog furnishes specs for modular dc open-frame and enclosed low voltage, and microprocessor power supplies, and introduces a miniature dc-dc converter. **Elexon Power Systems, Santa Ana, Calif.**
Circle 323 on Inquiry Card

Communications Line Monitor

Data sheet encompasses features, programming procedures, functional block diagrams, layout configurations, and specifications relevant to the Hawk 4000 datatrap. **International Data Sciences, Inc, Providence, RI.**
Circle 324 on Inquiry Card

Permanent Magnet Motors

Folder gives advantages, specs, performance characteristic curves, and dimensional drawings for M4000 series motors. **RAE Corp, McHenry, Ill.**
Circle 325 on Inquiry Card

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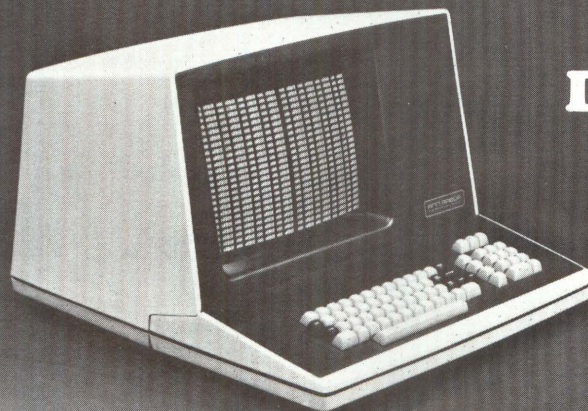
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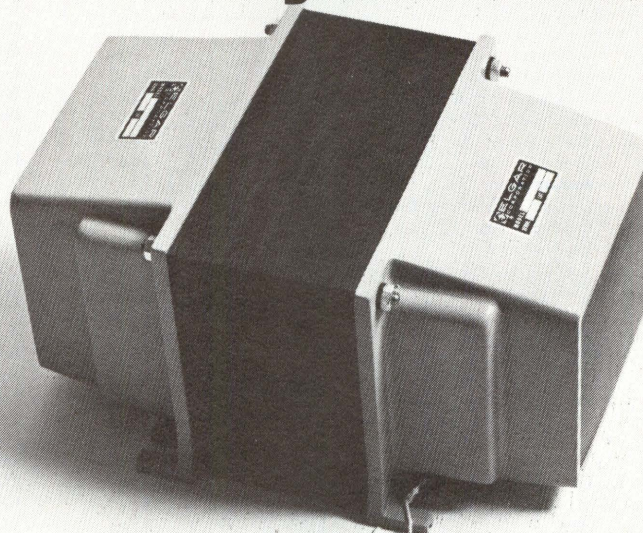
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